Universidad de Granada
Departamento de Electrónica y Tecnología
de Computadores

Advanced Simulation of Nanotransistors

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OUTLINE

1. Introduction. Why?
2. Simulation concepts & tools. How?
3. Simulation results. What?
    - A. Carrier mobility (electron & holes): ultrathin FDSOI, DGSOI, strained-Si channels, arbitrary crystallographic orientation
    - B. I-V characteristics of short channel devices. Radiation effects on FinFETs.
    - C. Si nanowires. Transport of 1D electron gases.
    - D. Design of new devices: A-RAM and A2RAM memory cells.

1.- Introduction.

- Why do we do simulation?
  - To have good friends

  - To attend conferences and publish papers

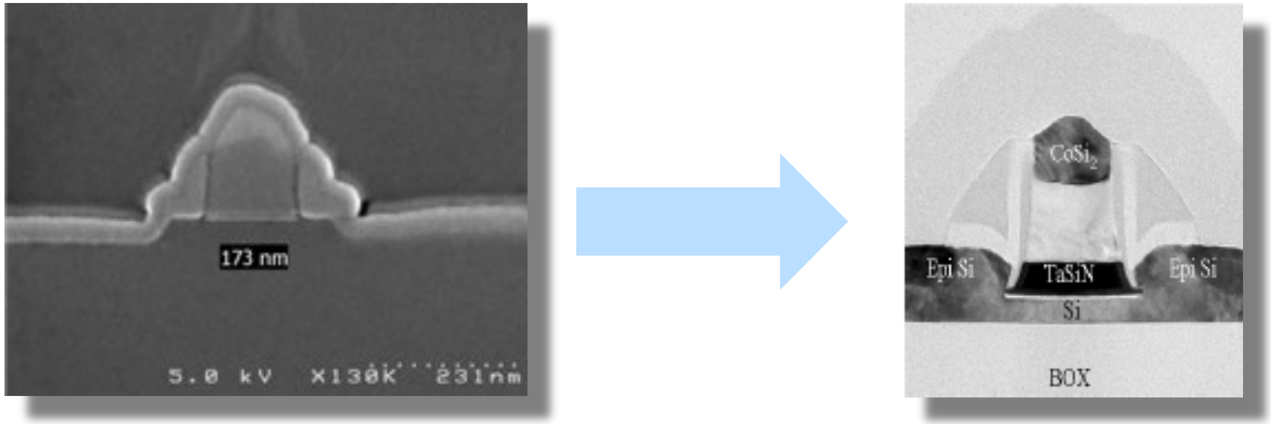
  - These are good reasons, of course, but there are others

1.- Introduction.

- Why do we do simulation?
  - If we want to use a device in a circuit, you need to understand how the device works !
  - If we want to improve the performance of a given device, you have to know how this device behaves internally!!
  - If you want to propose new devices to overcome the scaling limitations of existing technology, you have to demonstrate that the device works, and you have to optimize it, before fabrication.

  - But this is not easy nor evident with today's devices ! Which are today devices?

From doping based scaling to thickness based scaling



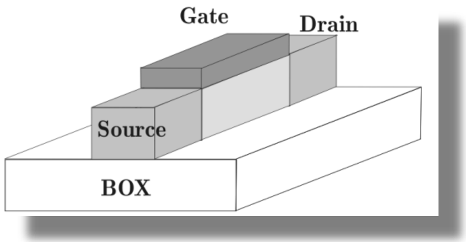
Following Moore's law: problems with non-trivial solution appear (high dopings, variability issues)

Reconsider the classical concepts

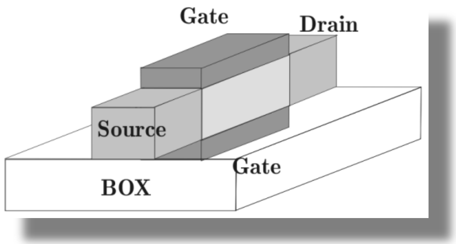
From doping based scaling to thickness based scaling

If one gate is not enough, why don't we have more than one?

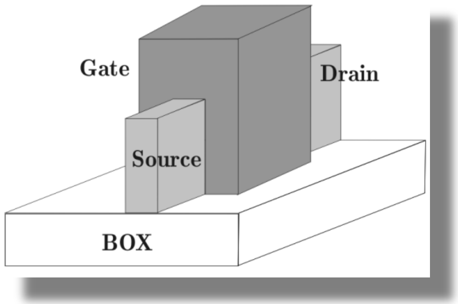
SOI



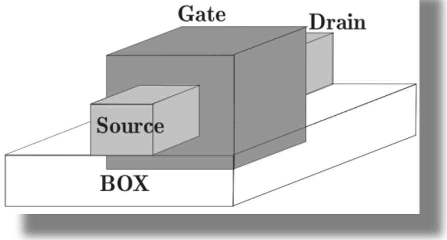
DG-SOI



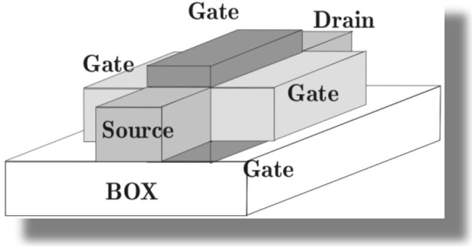
Fin FET



GAA



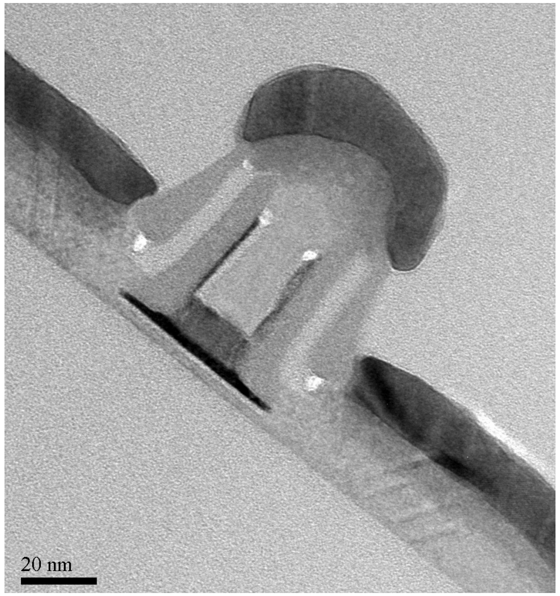
G^4-SOI



CMOS Scaling

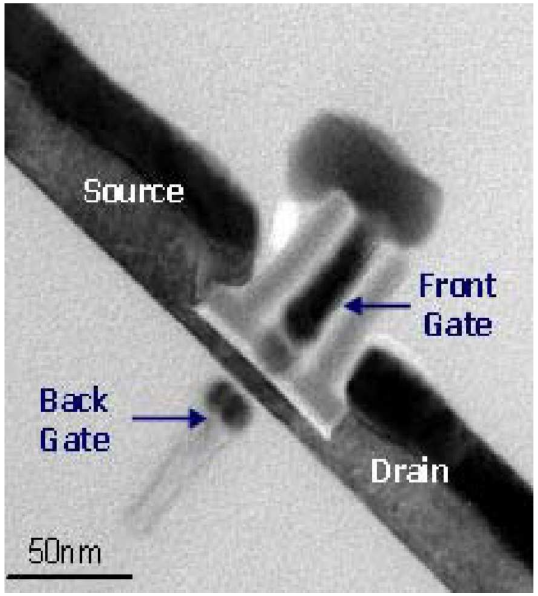
- **SOI: Thickness based & number of gates**

(Courtesy of LETI)



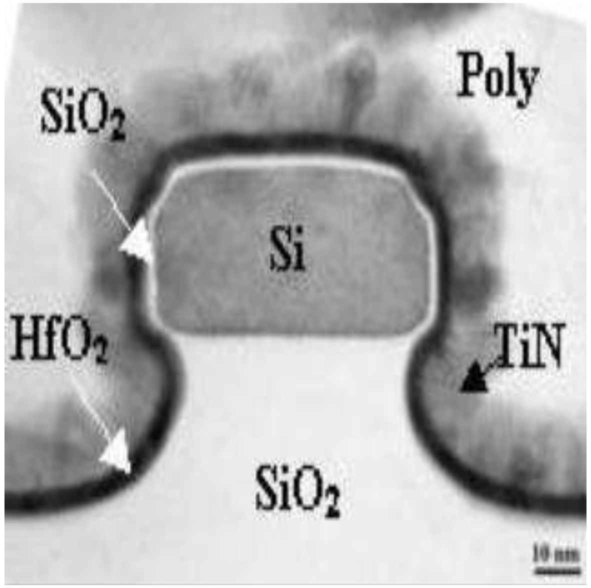
Planar FDSOI

$T_{Si} \approx L_G/4$



Double gate SOI

$T_{Si} \approx L_G/2$



Tri-Gate/FinFET

$T_{Si} \approx W \approx L_G$

More Moore

The continuous scaling of CMOS requires significant innovations:

1.- Multi-gate devices. → **better scaling.**

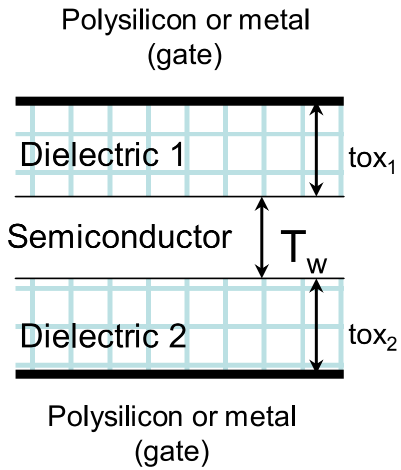
2.- Enhancement of carrier mobility:
   a. Specific doping profiles
   b. Lightly doped epitaxial layers
   c. Straine
   d. Crysta

Our goal:
Carrier mobility in multigate devices

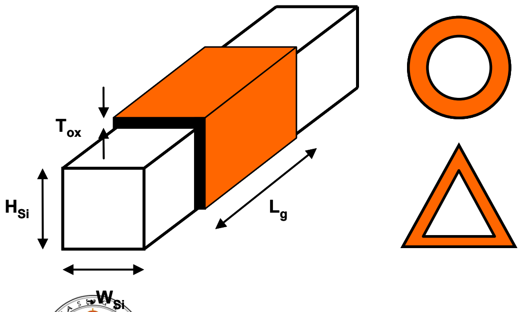
More Moore

We will consider two kind of devices:

1. Quantum-well devices:
   Carriers are confined in one dimension, but can drift in the other two.



2. Quantum-wire devices:
   Carriers are confined in two dimensions, and are drifted in the other dimension.

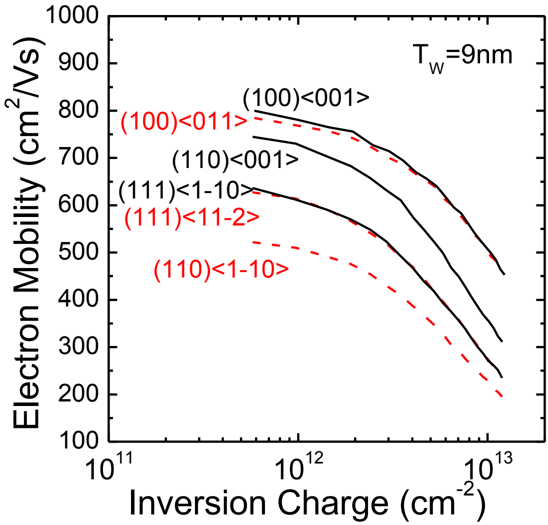


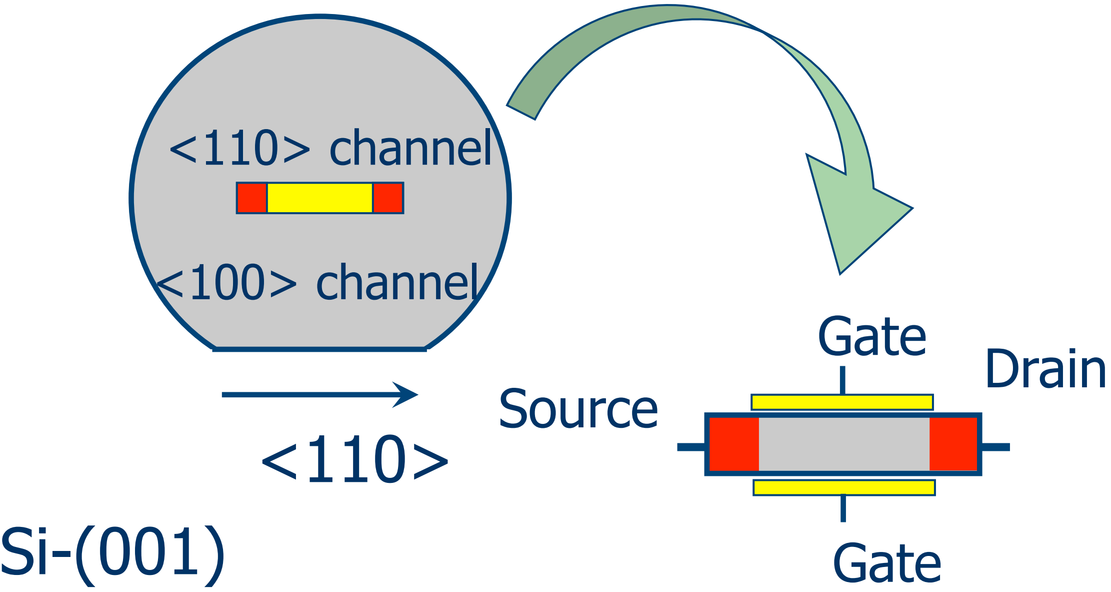
New simulation challenges

- It is not an easy task !!
- The new device structures require new simulation techniques and tools.
- Conventional tools are not accurate any more.
- Quantum effects become extremely important.
- New procedures are becoming necessary.

Simulation examples

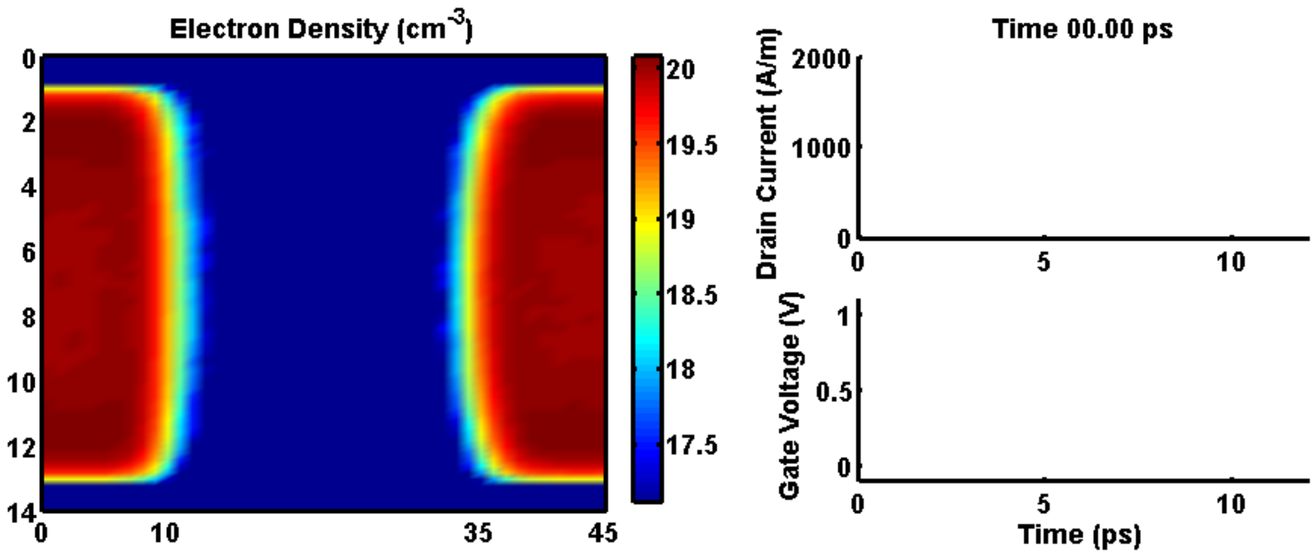
- Simulation of carrier transport in materials and devices.
  - ✓ Goal: simulate the behavior of electron devices, i.e.,
    1. Evaluate the transport properties of charge carriers in materials, or semiconductor structures: carrier mobility, velocity overshoot.





Simulation examples

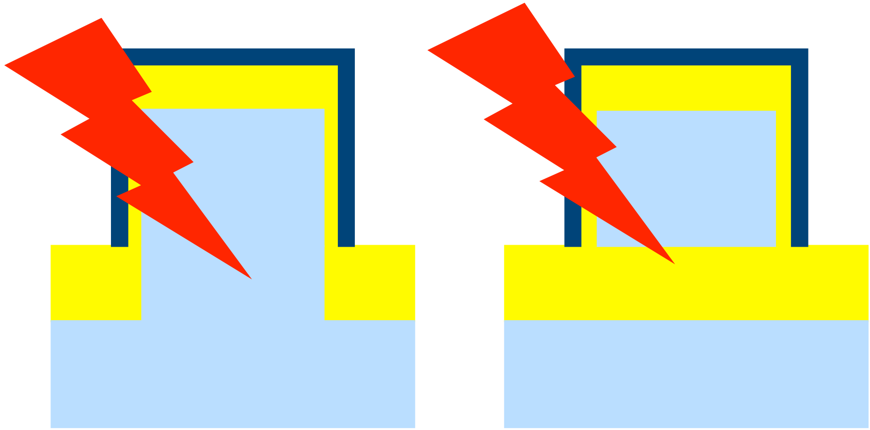
- Simulation of carrier transport in materials and devices.
  - ✓ Goal: simulate the behavior of electron devices, i.e.,
    2. Calculate the current at the terminals of a device, knowing the bias applied to them.



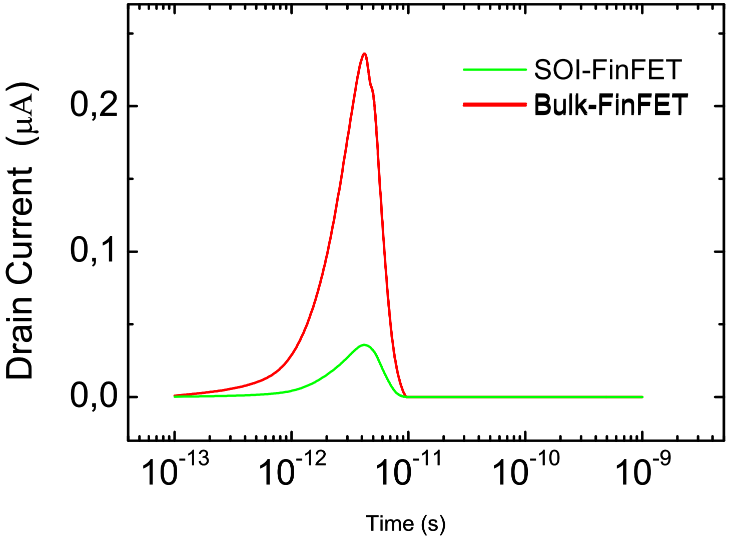
Simulation examples

- Simulation of carrier transport in materials and devices.
  - ✓ Goal: simulate the behavior of electron devices, i.e.,
    3. Understand device behavior under physical phenomena:

       FinFET on Bulk vs FinFET on SOI: radiation effects

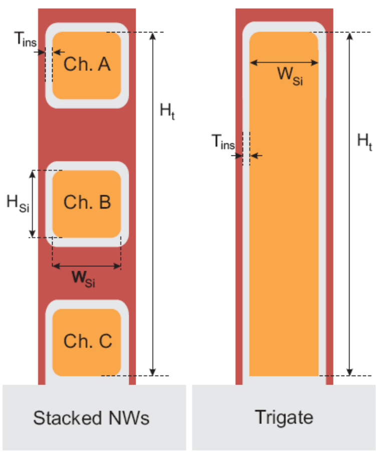


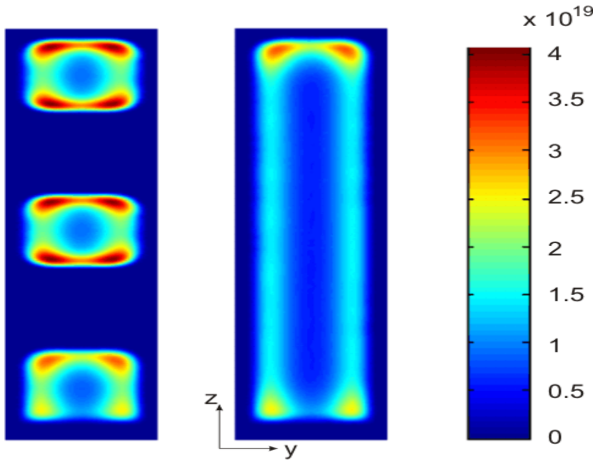
Bulk-FinFET SOI-FinFET

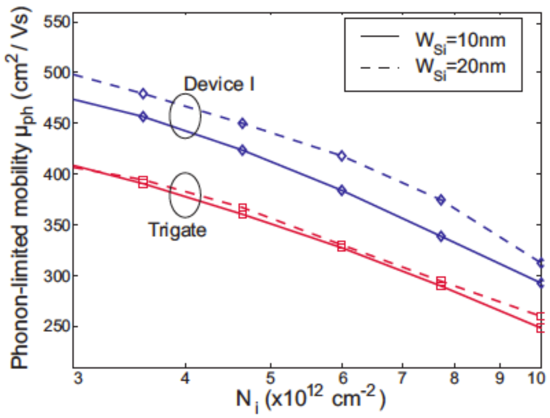


Simulation examples

- Simulation of carrier transport in materials and devices.
  - ✓ Goal: simulate the behavior of electron devices, i.e.,
    4. Simulation of Si-nanowires (too many unknowns)
       - ✓ Multigate devices → CMOS scaling
       - ✓ Different design alternatives: FinFETs, MC MOSFETs, GAAs, etc.



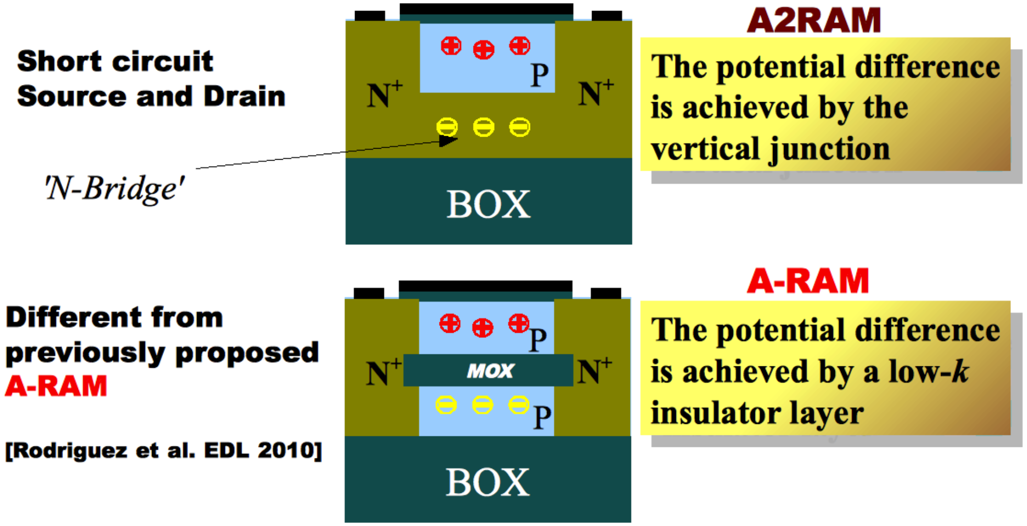




Simulation examples

- Simulation of carrier transport in materials and devices.
  - ✓ Goal: simulate the behavior of electron devices, i.e.,
    5. Design new devices: e.g. A-RAM and A2RAM memory cells

The Dual-Body concept



Short circuit Source and Drain

A2RAM

The potential difference is achieved by the vertical junction

Different from previously proposed A-RAM

[Rodriguez et al. EDL 2010]

A-RAM

The potential difference is achieved by a low-*k* insulator layer

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    3. Band structure. Electrons and holes.
    4. Transport properties. Scattering events. Carrier mobility. Mobility boosters.
    5. Device simulation.
3. Simulation results. What?

Simulation concepts

- An electron device is a system of many electrically charged particles that interact with an externally applied electric and magnetic fields and which each other.
- Particles are distributed both in geometrical and momentum space, following the particle distribution function:

$$f = f(r,k,t)$$

- The evolution of the particle distribution function is governed by the Boltzmann transport equation, BTE (semiclassical approximation):

$$\frac{\partial f}{\partial t} = -v \cdot \nabla f - \frac{1}{\hbar}\frac{\partial p}{\partial t} \cdot \nabla_k f + \left.\frac{\partial f}{\partial t}\right|_{coll}$$

Simulation concepts

- A closer look to BTE:

$$\frac{\partial f}{\partial t} = -v\cdot\nabla f - \frac{1}{\hbar}\frac{\partial p}{\partial t}\cdot\nabla_k f + \left.\frac{\partial f}{\partial t}\right|_{coll}$$

the group velocity of the carriers, $v = (1/\hbar)\nabla_k E(k)$,
E(k) being the dispersion relation, which takes into account the periodic potential of the crystal.

Simulation concepts

- A closer look to BTE:

$$\frac{\partial f}{\partial t} = -v\cdot\nabla f - \frac{1}{\hbar}\frac{\partial p}{\partial t}\cdot\nabla_k f + \left.\frac{\partial f}{\partial t}\right|_{coll}$$

the second term represents the acceleration driven by the Lorentz force:

$$\frac{\partial \vec{p}}{\partial t} = e\left(\vec{F} + \vec{v}\times\vec{B}\right)$$

the third term represents the changes because of scattering:

$$\left.\frac{\partial f}{\partial t}\right|_{coll} = \sum_{k'}\left[f\left(r,k',t\right)W\left(k',k\right) - f\left(r,k,t\right)W\left(k,k'\right)\right]$$

Simulation concepts

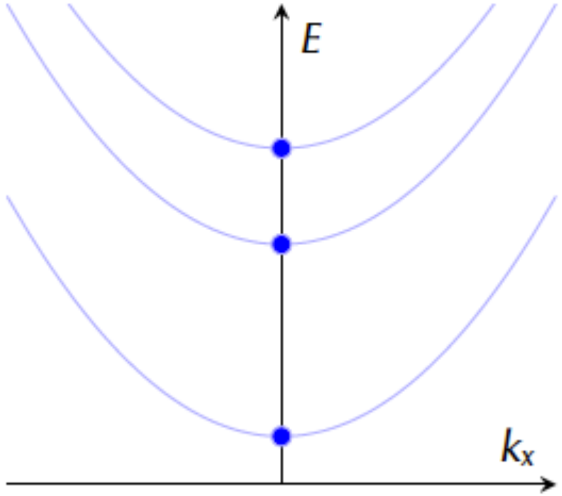
- To solve Boltzmann Transport Equation we need:
  1. Band structure of the device (not of the material)
  2. Electric and magnetic fields that carriers “see”
  3. Scattering mechanisms:
     1. Phonon scattering
     2. Surface roughness scattering
     3. Coulomb scattering

Simulation concepts

- Bandstructure of the device:

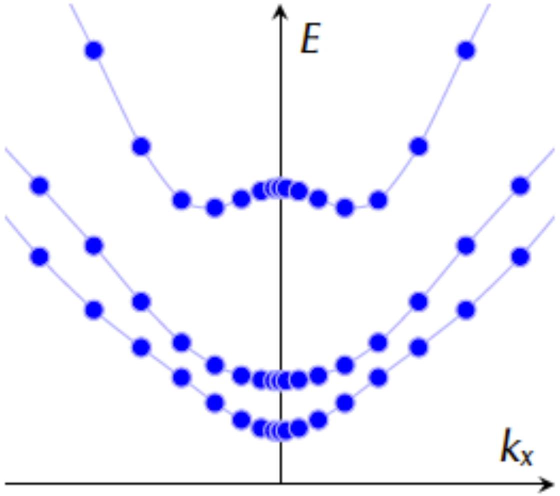
  1. Analytical description, Effective Mass Approximation
  2. k•p method
  3. Tight Binding
  4. Pseudopotentials
  5. Ab-initio calculations

Simulation concepts


Electrons

$$E = E_i + \frac{\hbar^2 k_x^2}{2m_x}$$

The subband energy is built from the minimum using a parameter


Holes

interpolation: $E = E_i(k_x)$

The energy of the subband has to be calculated for every k_x

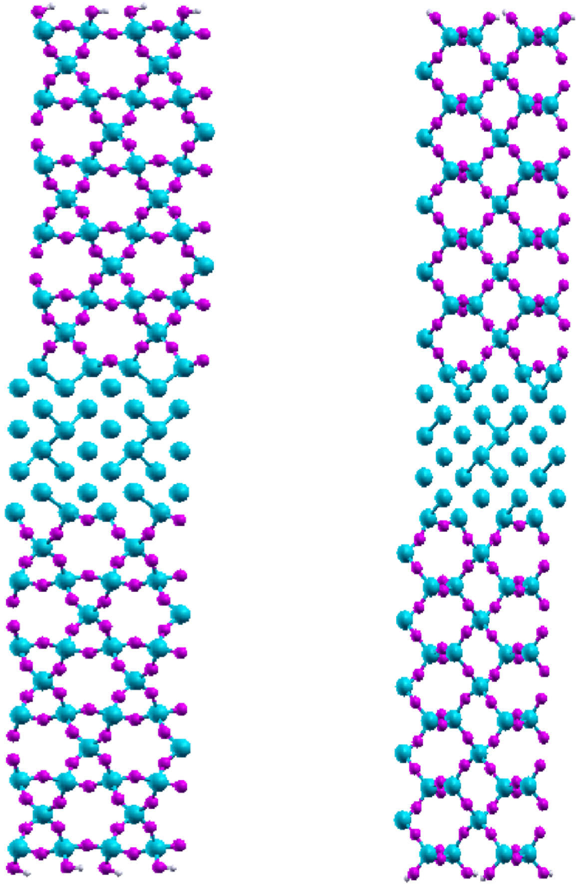
Simulation concepts

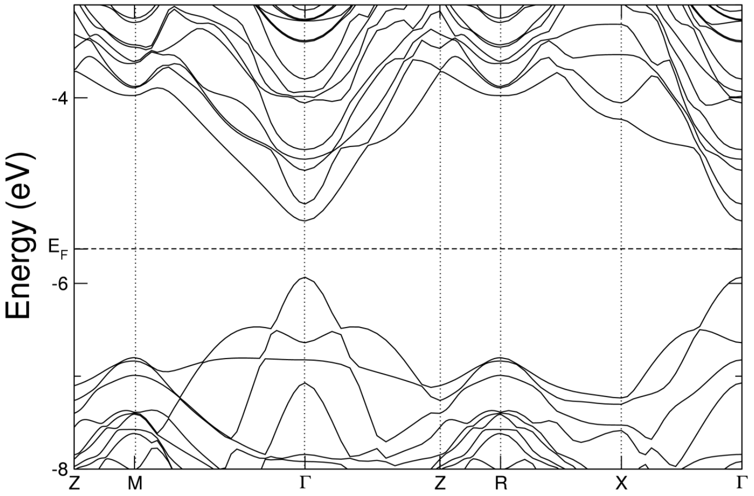
- Bandstructure of the device:

  1. Analytical description, Effective Mass Approximation
  2. k•p method
  3. Tight Binding
  4. Pseudopotentials
  5. Ab-initio calculations

Simulation concepts

- Bandstructure of a DGSOI transistor (ab-initio):





Possibility to study atomic-scale phenomena: dopants, dislocations, etc.

Simulation concepts

- A closer look to BTE:

$$\frac{\partial f}{\partial t} = -v \cdot \nabla f - \frac{1}{\hbar}\frac{\partial p}{\partial t} \cdot \nabla_k f + \left.\frac{\partial f}{\partial t}\right|_{coll}$$

From f(r,k,t) we can evaluate all the variables of interest:

$$n(\vec{r},t) = \frac{1}{V}\sum_k f(\vec{r},\vec{k},t)$$

$$\vec{J}_n(\vec{r},t) = \frac{e}{V}\sum_k \vec{v}(\vec{k}) f(\vec{r},\vec{k},t)$$

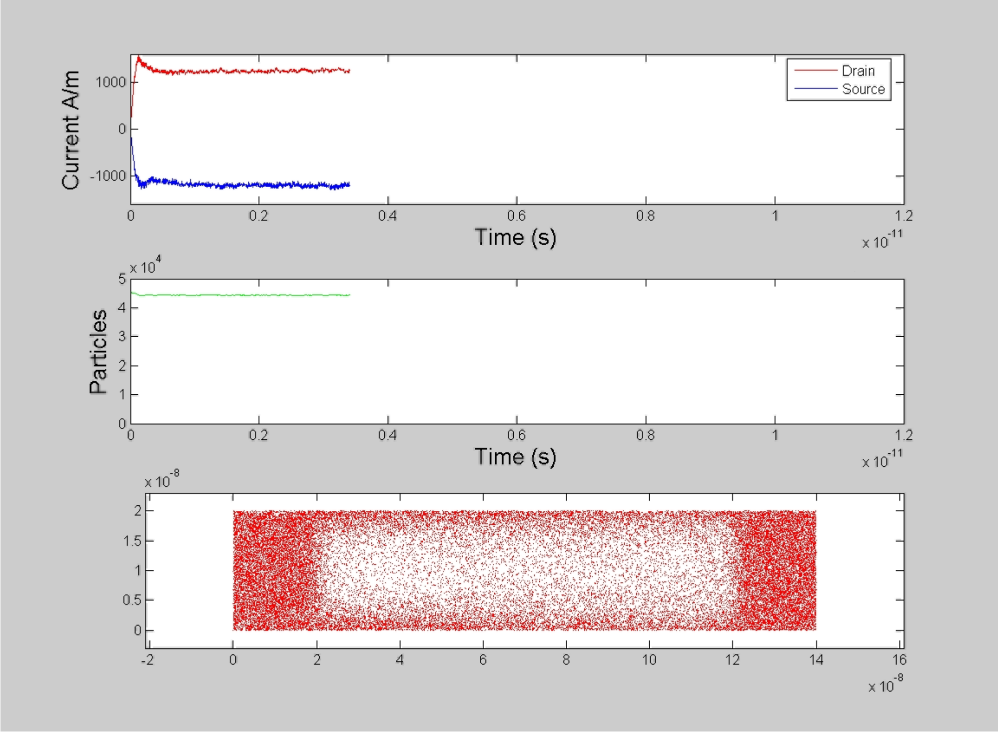
Simulation concepts

- Our goal is then to solve BTE. However,
- The solution of the BTE for realistic devices is a very difficult task
- Difficulties arise from:
    1. Non homogeneous device structure (doping and topology).
    2. Models for scattering mechanisms.
    3. Complexity of the band structure.

- Most common solutions: statistical methods (Monte Carlo) or drastic approximations (methods of moments: drift-diffusion and hydrodynamic method).
- We have applied the Monte Carlo method to solve the Boltzmann transport equation in advanced devices.

The Ensemble Monte Carlo method

- We assume that the charged particles move inside the semiconductor structure undergoing a succession of free flights followed by scattering events:



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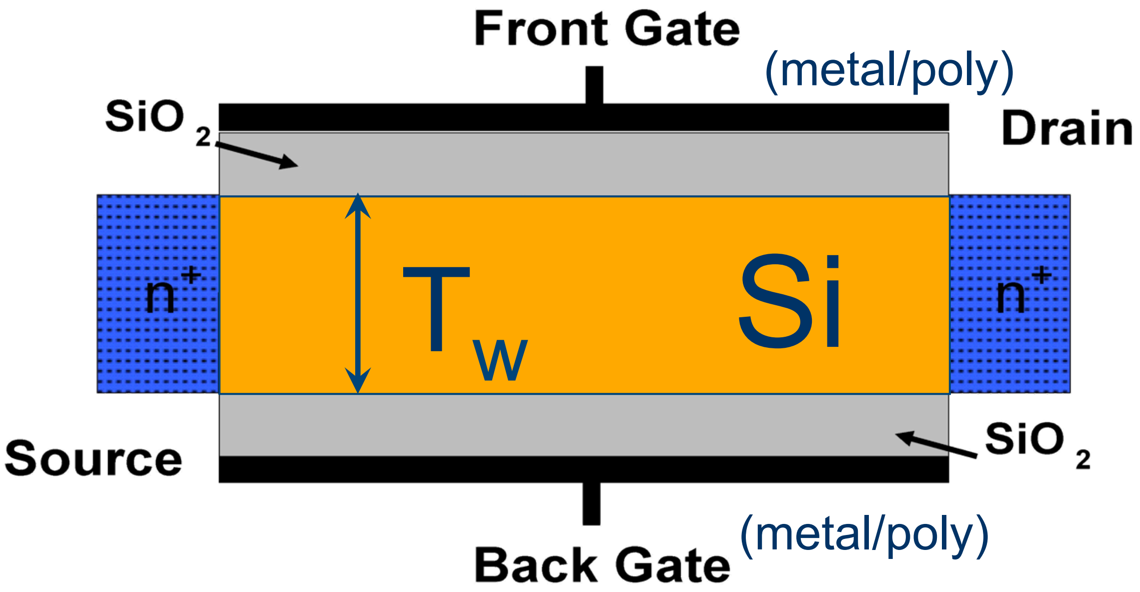
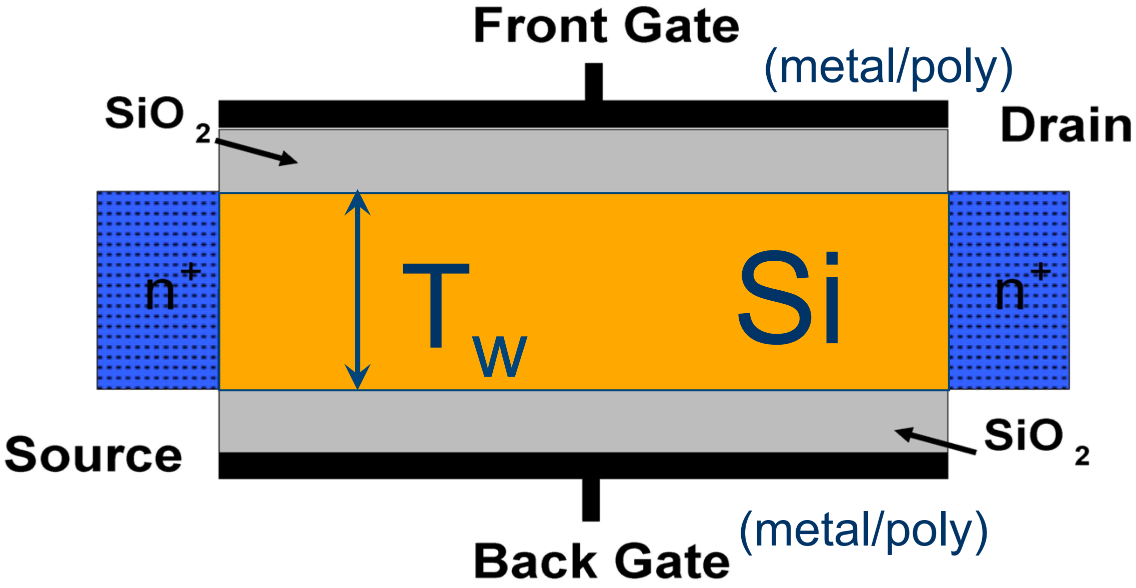
Double-Gate MOSFETs



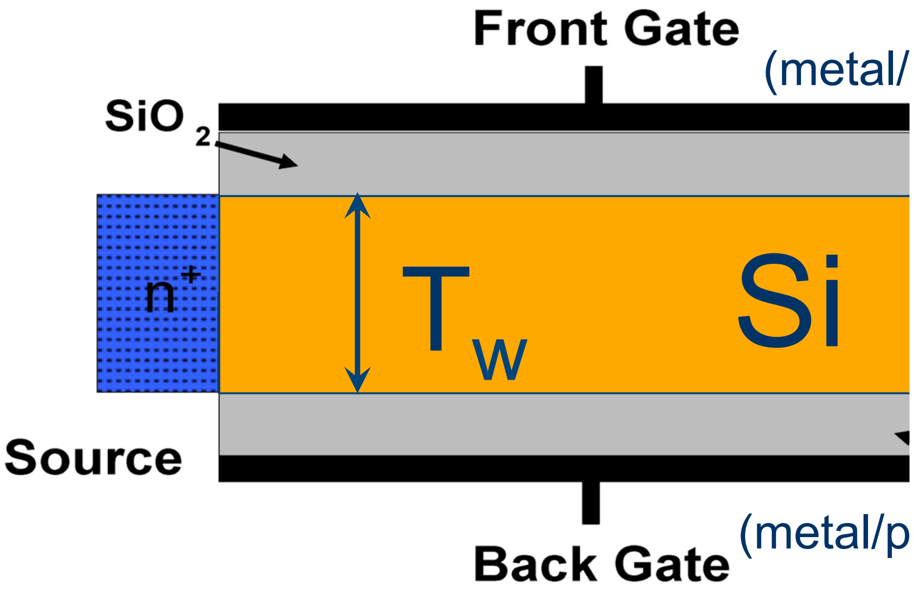
- Gate oxide: SiO_2 or high-k
- T_W: **50 nm to 1.5 nm**.
- Silicon layer undoped.
- N^+-Poly or midgap metal gates

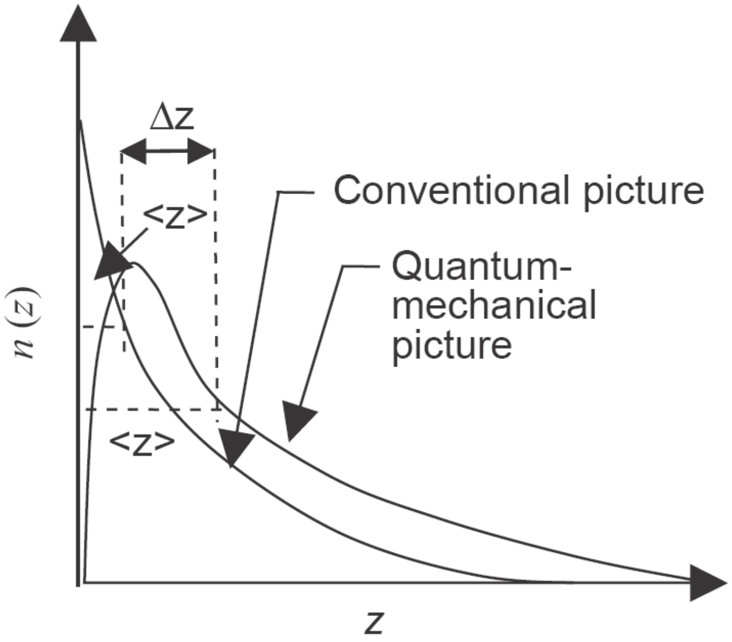
Double-Gate MOSFETs



- Silicon thickness becomes comparable to the De Broglie wavelength of carriers: Carriers become quantized in the direction perpendicular to the silicon thickness, T_W

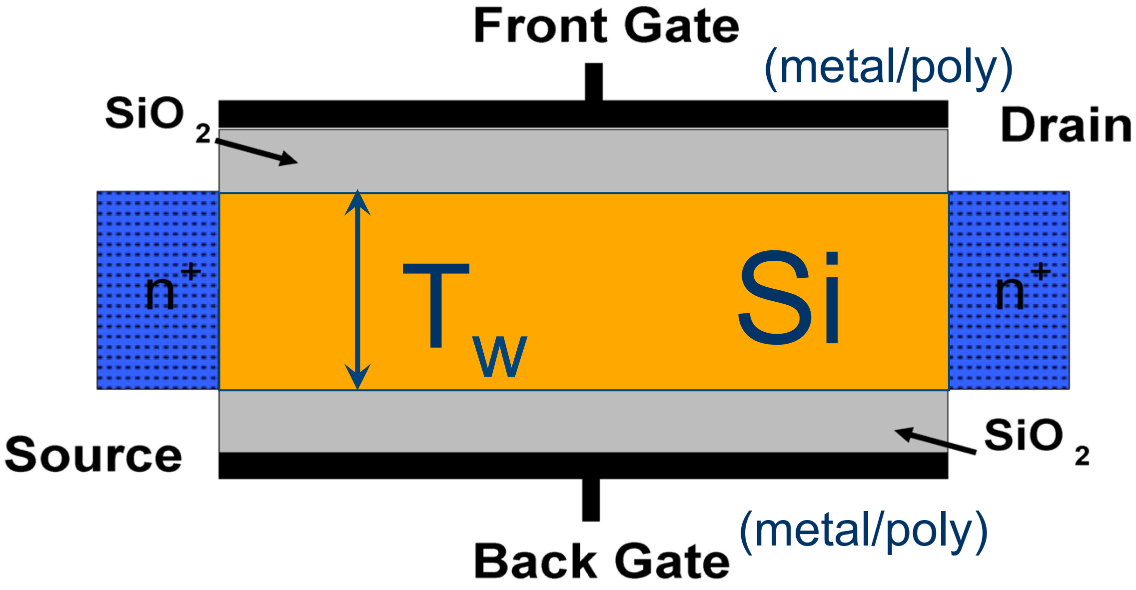
Double-Gate MOSFETs





- We have to self-consistently solve the Poisson and Schroedinger equations to calculate the distribution of the carriers in the structure.

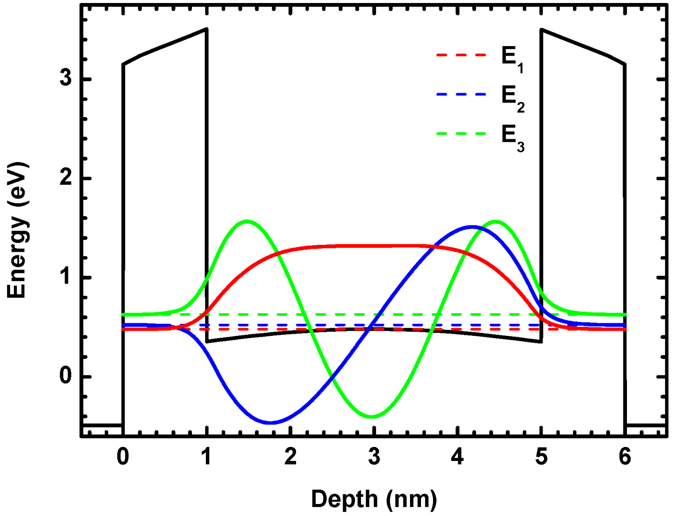
Double-Gate MOSFETs



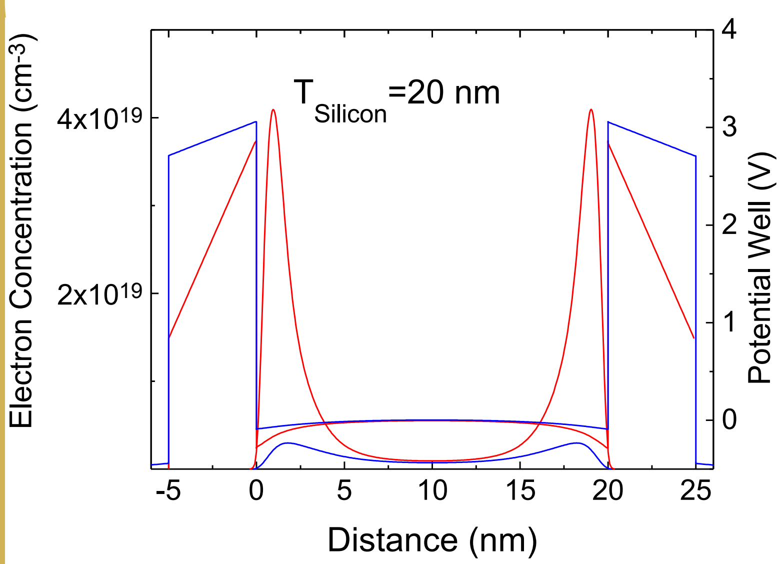
- Under the assumption of very long channel device:

$$-\frac{\hbar^2}{2m_z}\frac{d^2\psi_i}{dz^2} - e\phi(z)\psi = E_i\psi_i$$

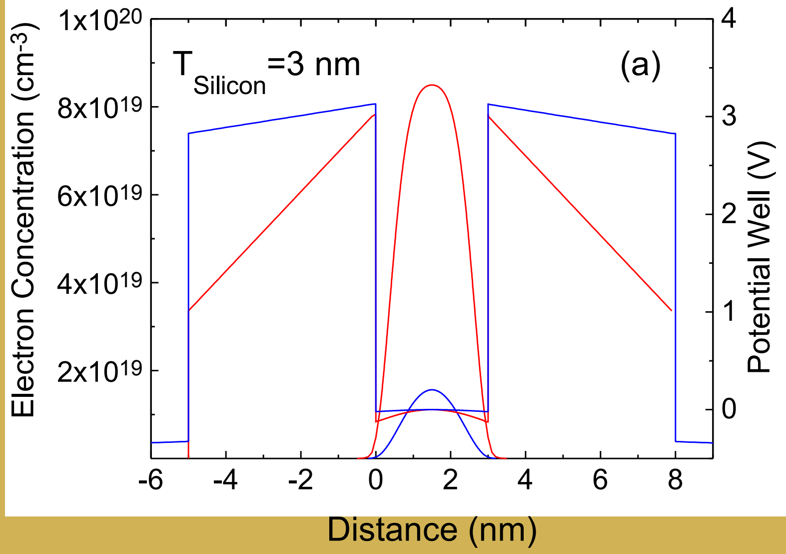
$$\frac{d^2\phi}{dz^2} = -\frac{1}{\varepsilon_{Si}}\sum_i n_i|\psi_i|^2$$



Double-Gate MOSFETs



- *Two channels connected in parallel*
  - Carriers are confined near each Si/SiO_2 interface.



- *Volume inversion*
  - Carriers are no longer confined at one interface but distributed throughout the entire silicon film

$$N_{inv} = 1.3\times10^{12}\,cm^{-2} \quad \text{(blue line)}$$

$$N_{inv} = 8.5\times10^{12}\,cm^{-2} \quad \text{(red line)}$$

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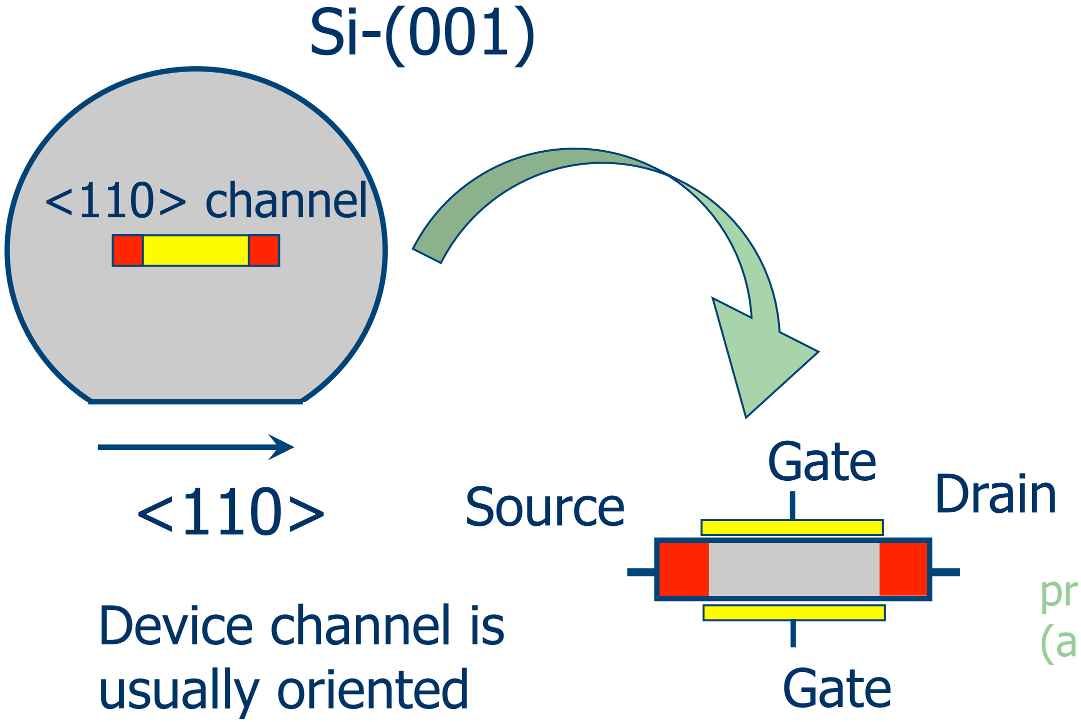
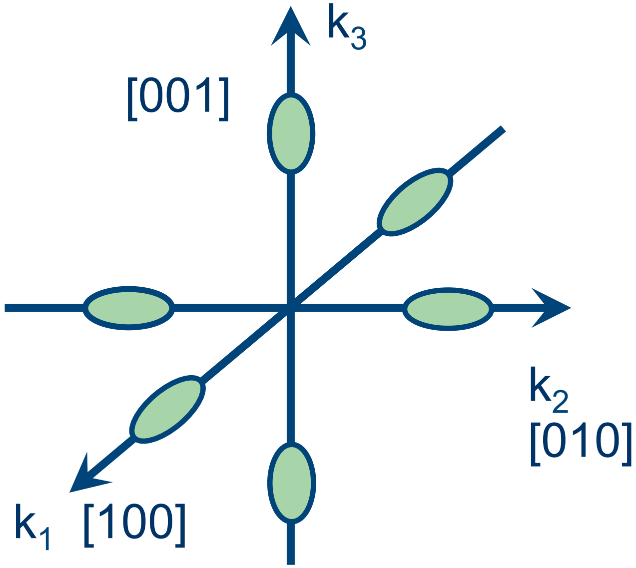
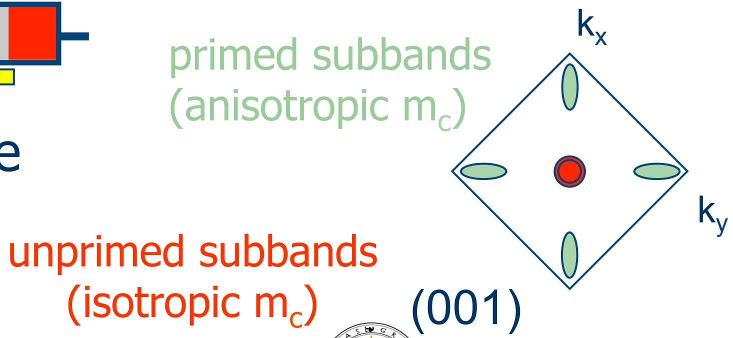
Double-Gate MOSFETs

- In conventional planar Si technology, (001) crystal orientation is generally used for MOSFETs.





Device channel is usually oriented parallel to the primary flat.

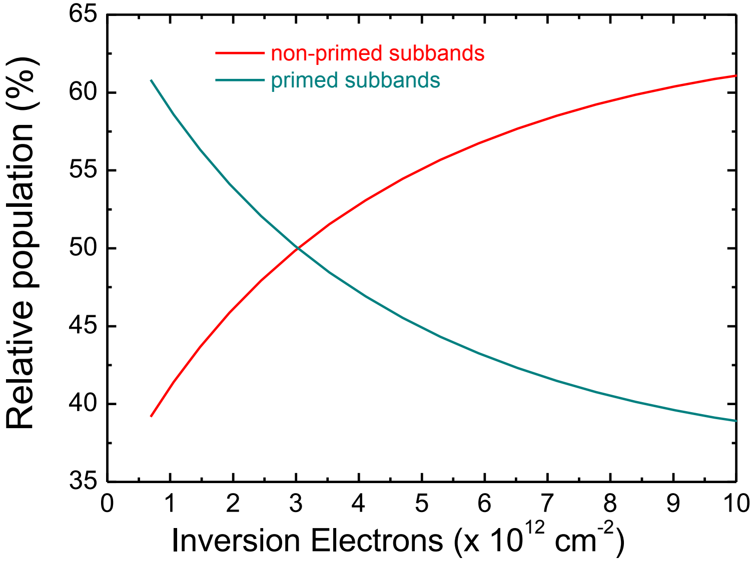


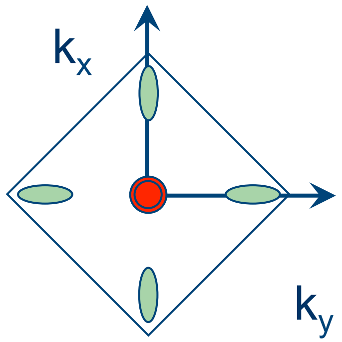
Double-Gate MOSFETs

- In conventional planar Si technology, (001) crystal orientation is
  MOSFETs :

Si-(001): Quantization splits Si-
degeneration:

1. Two lower valleys wit
   m$_c$) (unprimed subba
2. Four higher valleys wit
   m$_c$) (primed subbands





(001)

$m_{<100>} = m_t$

$m_{<010>} = m_t$

$n_v = 2$

$m_{<100>} = m_l$

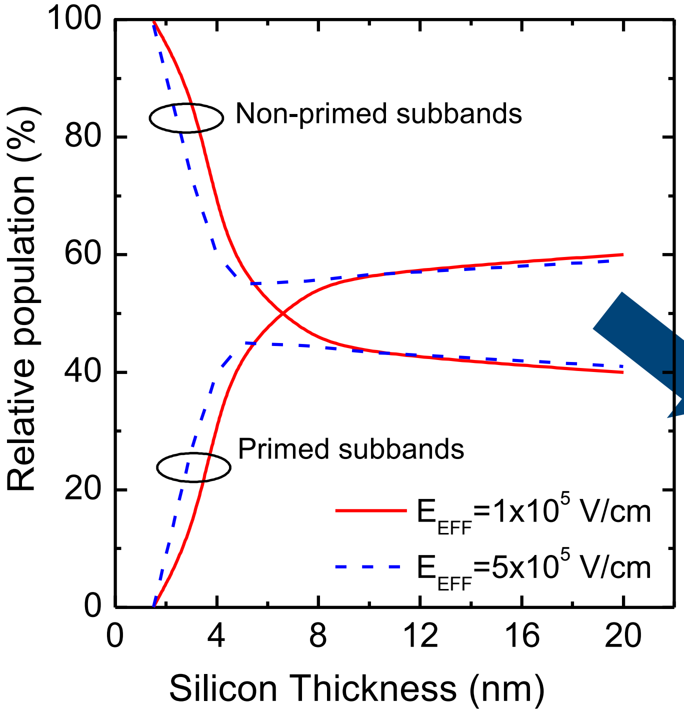
$m_{<010>} = m_t$

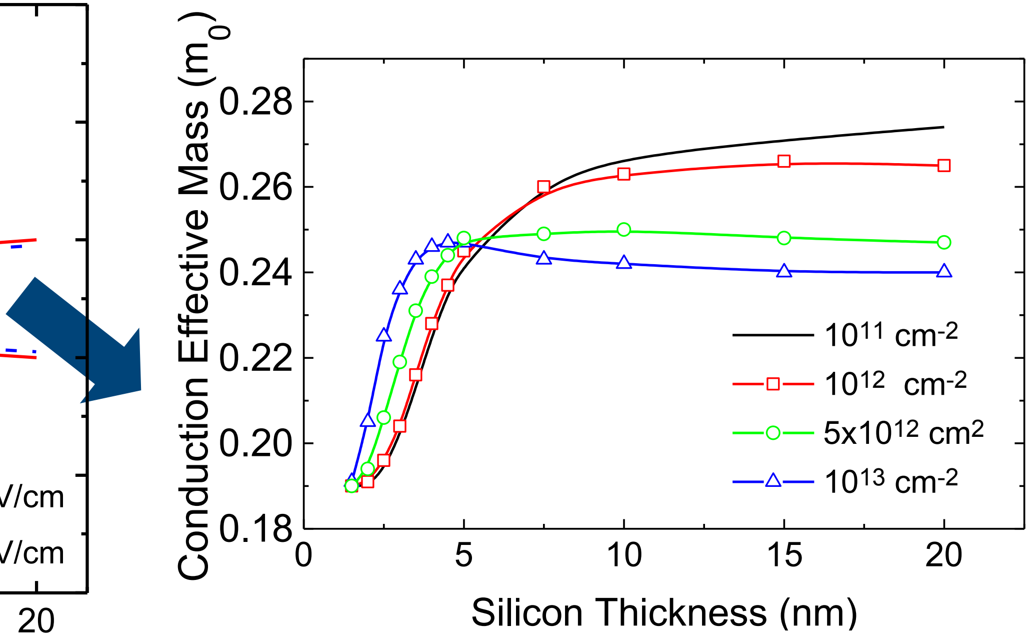
$n_v = 4$

Volume inversion

A-1) *Subband Modulation Effect*

Redistribution of subband population



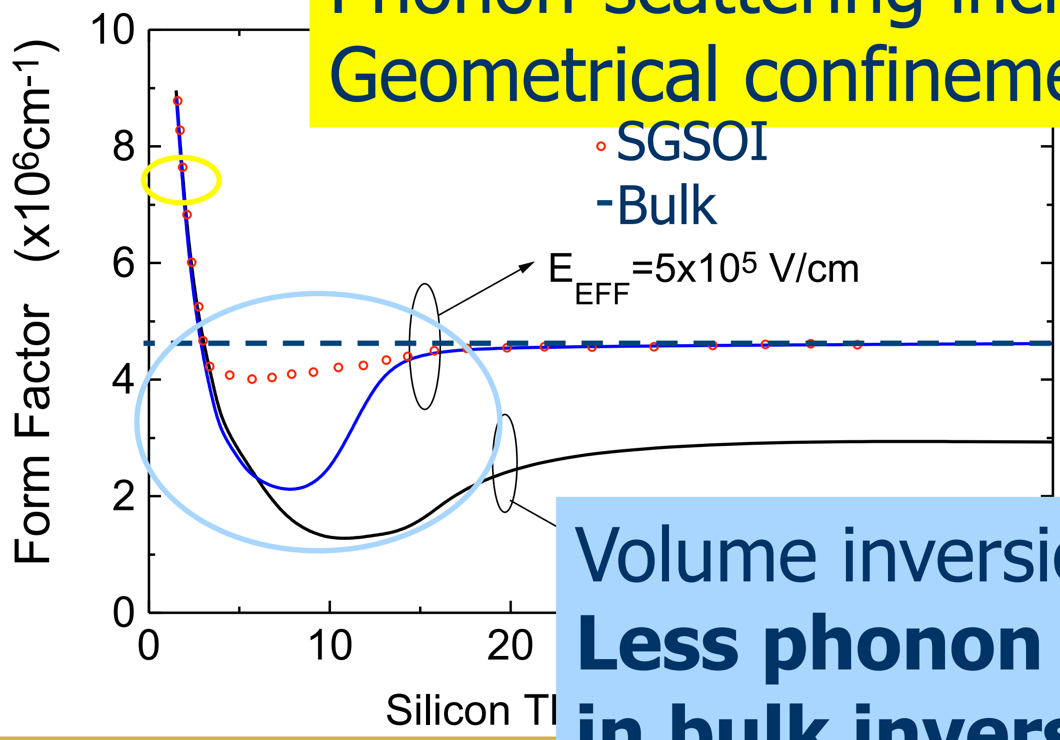


Reduction of conduction effective mass

Volume inversion

A-2 *Phonon scattering limitation*

Volume inversion makes that in the range 25-10 nm phonon scattering decreases instead of increasing as expected



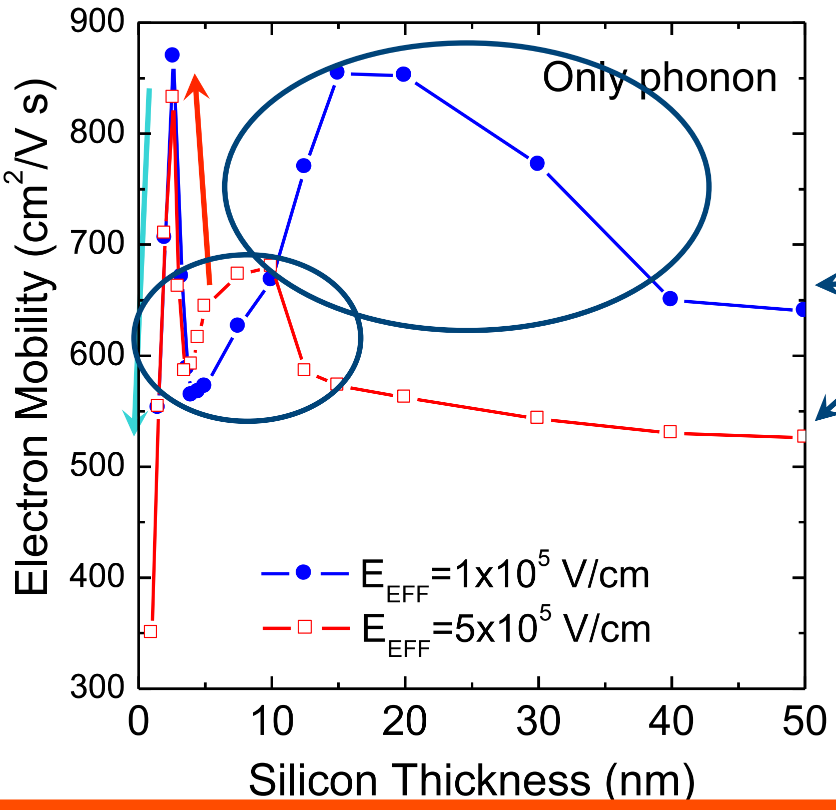
Phonon-scattering increase.
Geometrical confinement

$$I_{\mu\nu} = \int \left|\psi_\mu(z)\right|^2 \left|\psi_\nu(z)\right|^2 dz$$

Volume inversion effect.
Less phonon scattering than in bulk inversion layers

Electron Mobility

- PHONON SCATTERING (I)



Volume Inversion

Subband Modulation

Bulk MOSFET

Phonon Increase

Electron mobility is higher than in bulk silicon inversion layers

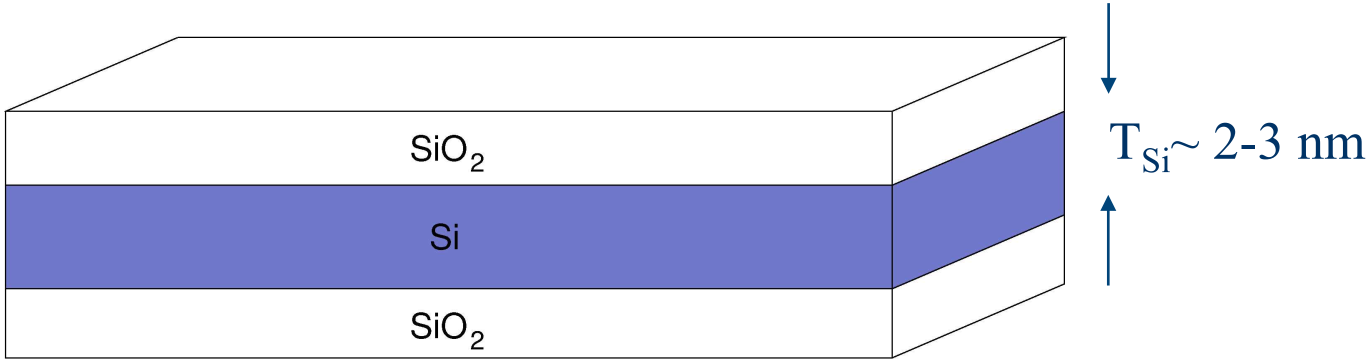
In addition to a better control of SCE, we have higher μ !!

Electron Mobility

- PHONON SCATTERING (II)

Bulk phonon model assumes an infinite silicon layer.

Are bulk phonons still appropriate for the simulation of ultrathin SOI devices?



Acoustic phonon model

- Phonons are modeled as elastic waves in an isotropic finite medium

$$\frac{\partial^2 \mathbf{u}}{\partial t^2} = s_t^2 \nabla^2 \mathbf{u} + (s_l^2 - s_t^2)\nabla(\nabla \mathbf{u})$$

- Simplified structure: single Si layer

- The solutions are:

$$u(r_\parallel, z) = w_n(q_\parallel, z)\, e^{i q_\parallel \cdot r_\parallel - i\omega_n t}$$

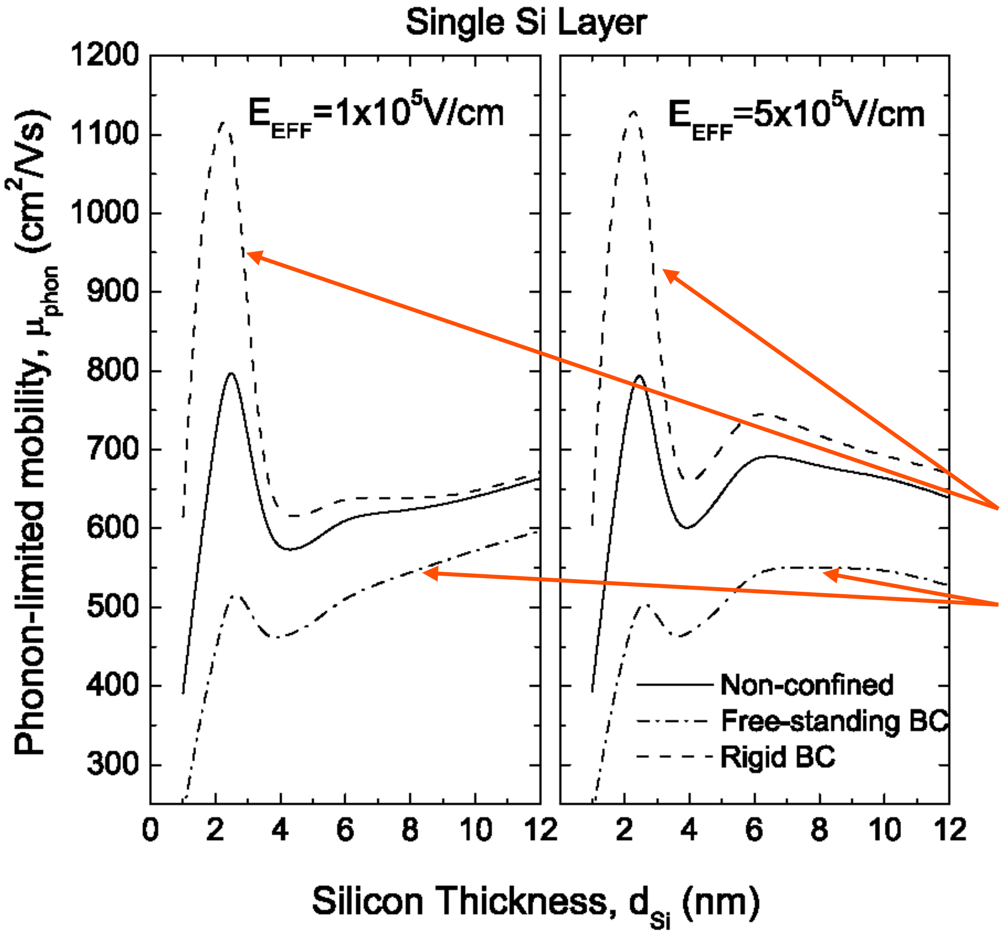
+ boundary conditions (BC) on exter

Quantization of phonons

- ✓ Free boundary conditions (vanishing stress tensor)
- ✓ Rigid boundary conditions (vanishing displacement u)

Acoustic phonon model

Electron mobility



Important effect of phonon confinement on electron mobility

rigid BC ⇒ mobility increase

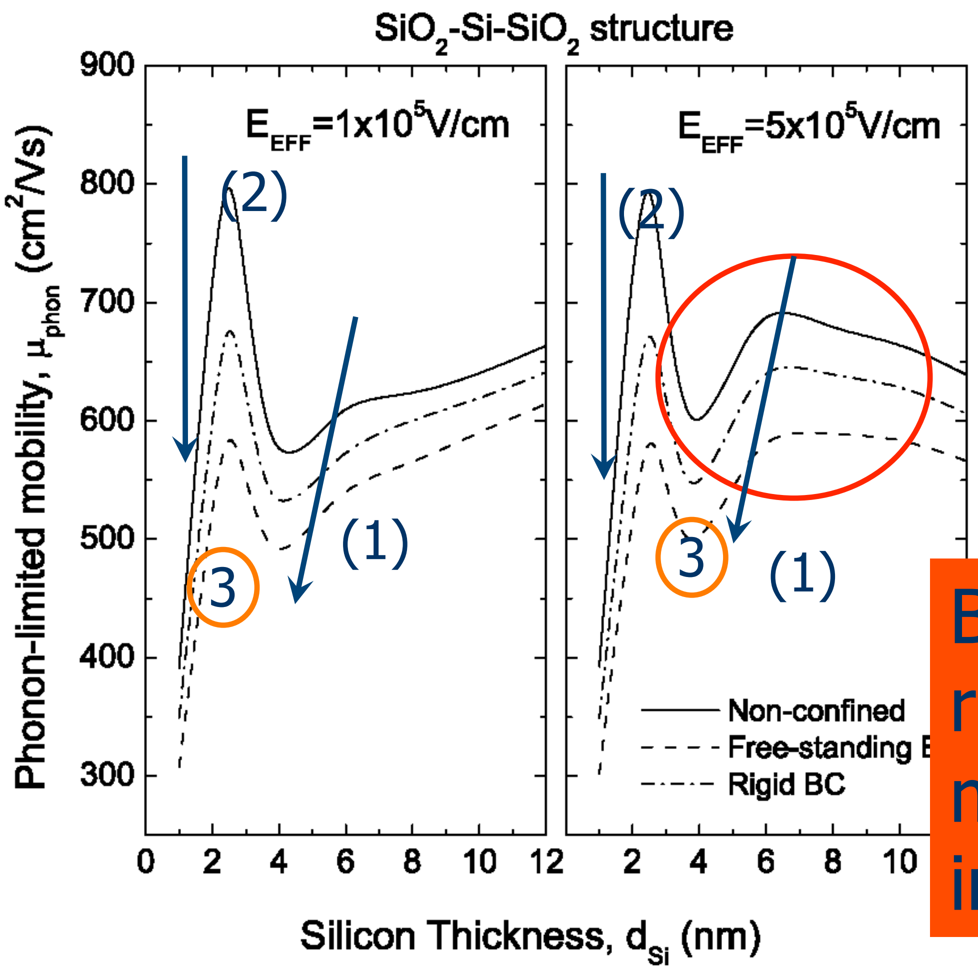
free BC ⇒ mobility decrease

Acoustic phonon model

- Phonon confinement and quantization are reproduced
- Phonon confinement has a strong effect on the mobility
- ... but we need more realistic boundary conditions !!

We consider an improved structure

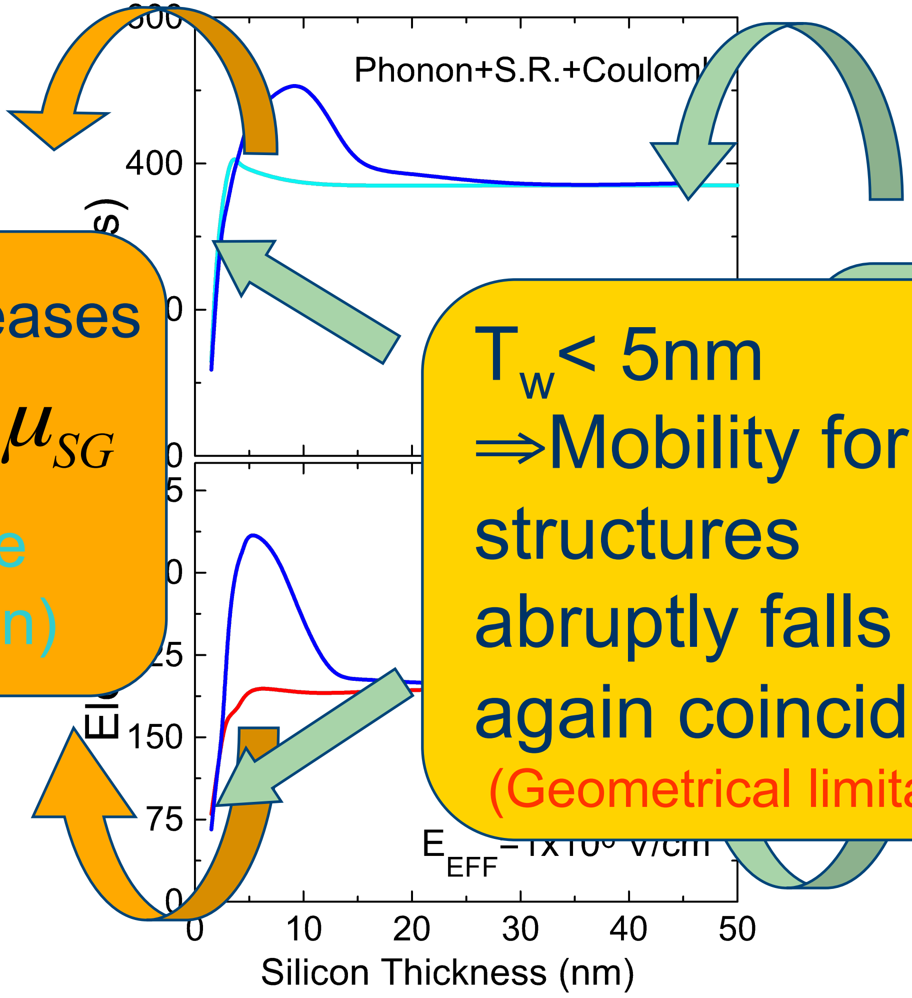
Acoustic phonon model



1. Both BCs imply an important electron mobility degradation.
2. The mobility peak around 2-4 nm is strongly suppressed

But, there is still a region where electron mobility is higher than in bulk inversion layers

Double Gate vs Single Gate



As T$_w$ decreases

⇒ $\mu_{DG} > \mu_{SG}$

(Volume inversion)

T$_W$< 5nm

⇒Mobility for both structures abruptly falls and again coincides.

(Geometrical limitations)

0 nm

y for

ctures

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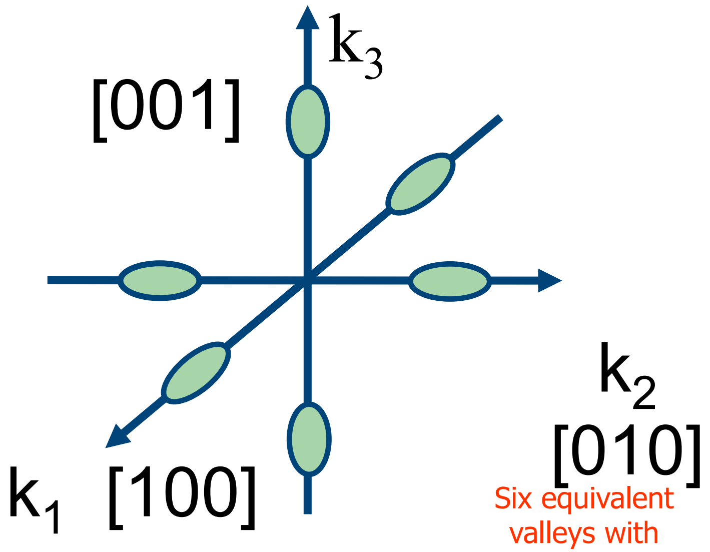
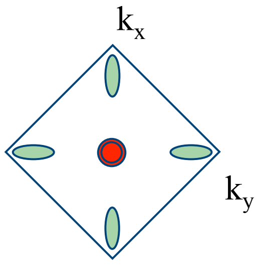
Crystallographic orientation

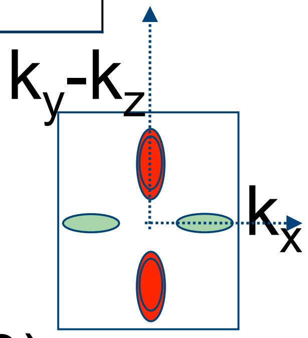
Quantization direction	m_3	n_v
(100)	0.916	2
	0.19	4
(110)	0.315	4
	0.19	2
(111)	0.258	6



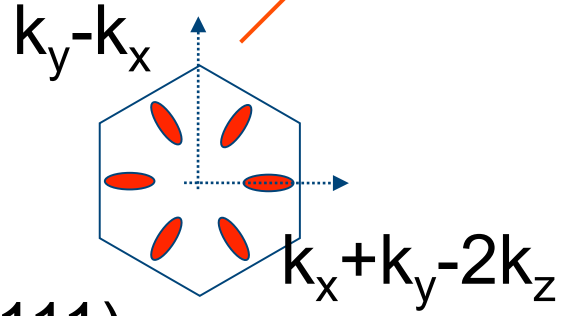
Six equivalent valleys with anisotropic m_c



(001)



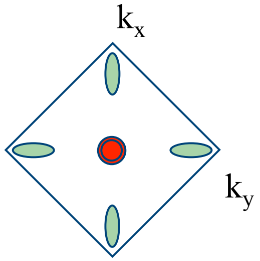
(110)



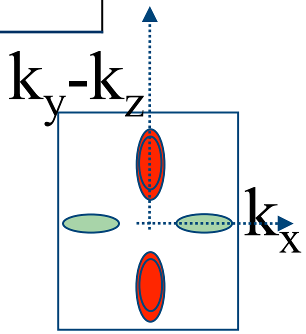
(111)

Crystallographic orientation

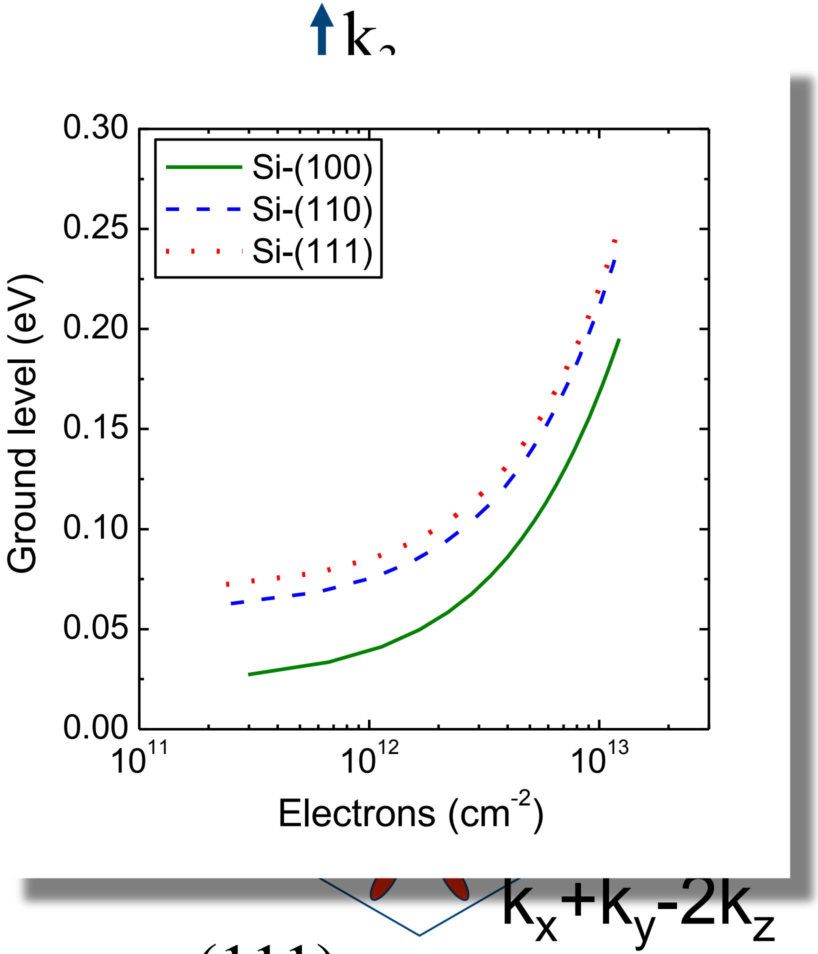
Quantization direction	m_3	n_v
(100)	0.916	2
	0.19	4
(110)	0.315	4
	0.19	2
(111)	0.258	6



(001)



(110)



(111)

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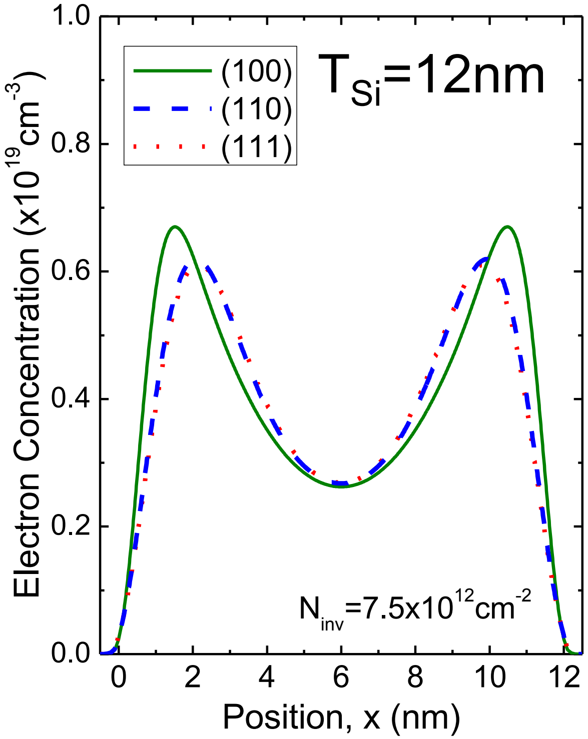
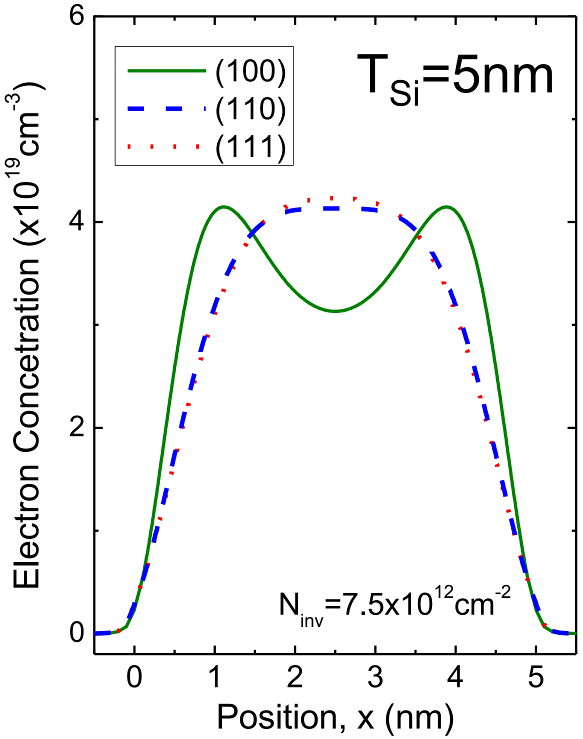
Crystallographic orientation

The higher quantization mass in the Si-(100) quantization orientation produces lower subband-energy levels → electrons are more confined to the Si/SiO_2 interfaces





Electrons in Si-(110) and Si-(111) are more spread into the silicon layer

Less effect of surface scattering mechanisms

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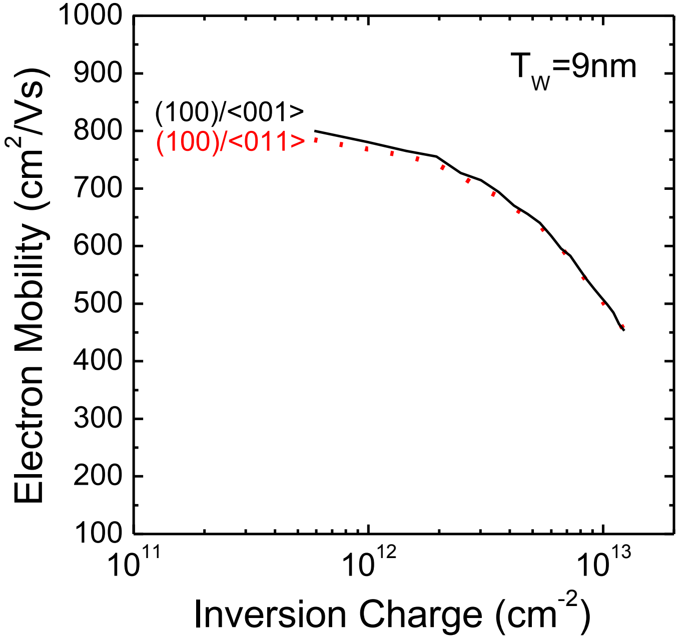
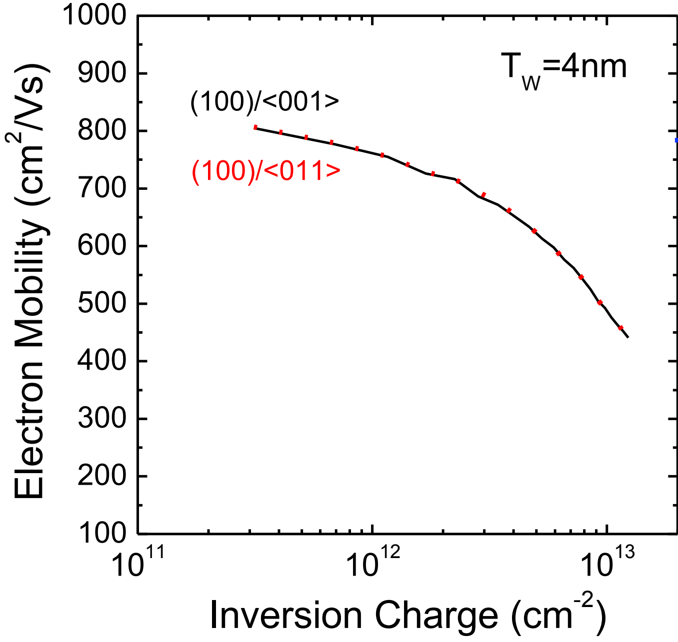
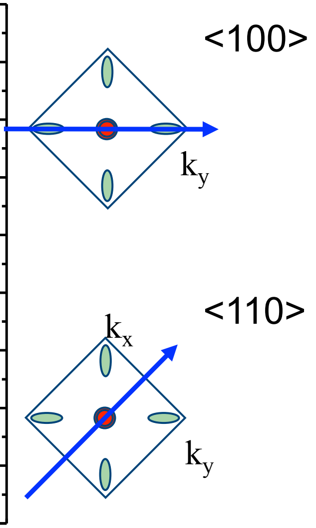
Crystallographic orientation

Monte Carlo calculation using phonon scattering and surface roughness scattering



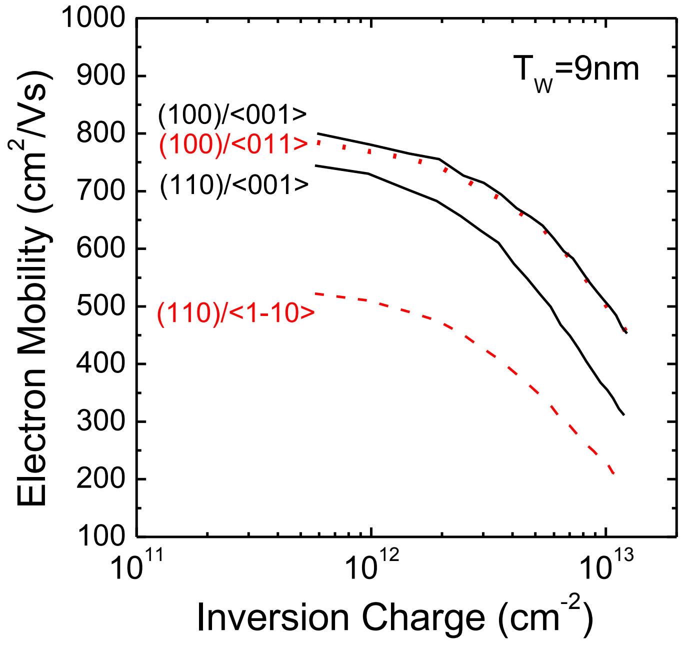


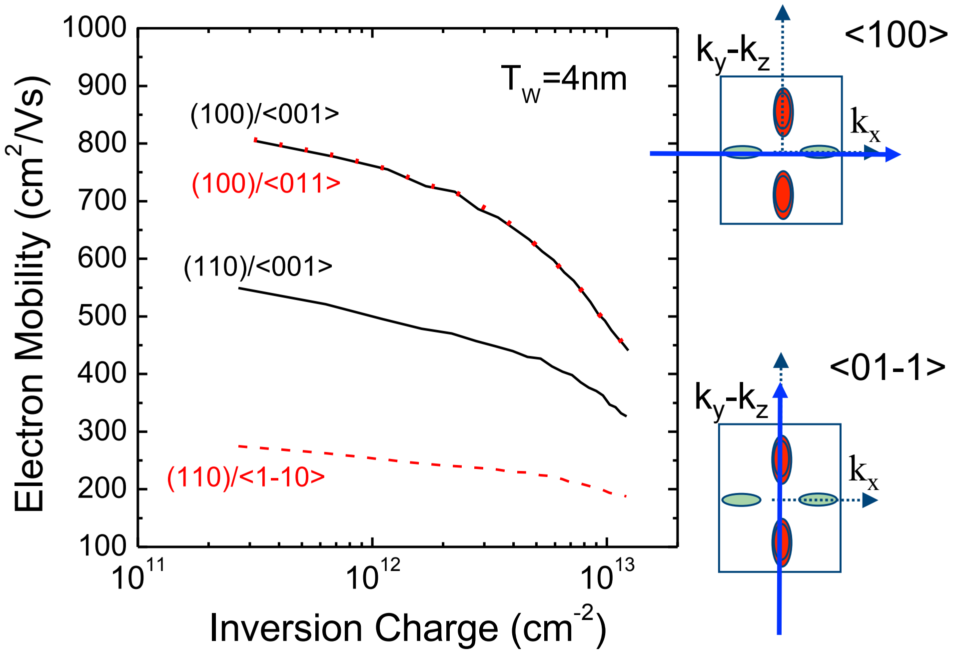


Crystallographic orientation

Monte Carlo calculation using phonon scattering and surface roughness scattering

The effects of the surface orientation are more important as the silicon thickness decreases

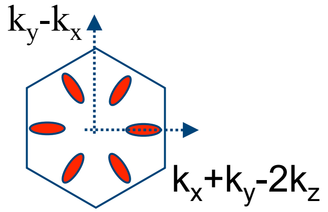


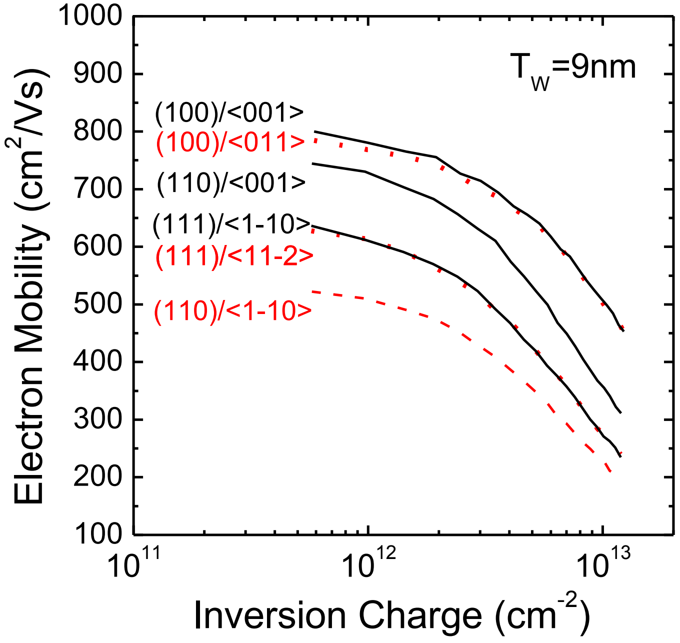


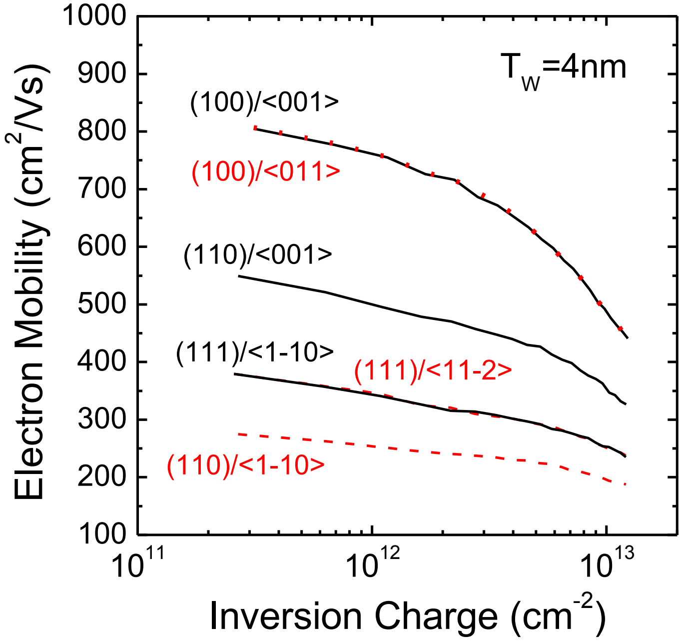
Crystallographic orientation

Monte Carlo calculation using phonon scattering and surface roughness scattering

The effects of the surface orientation are more important as the silicon thickness decreases



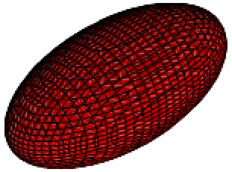




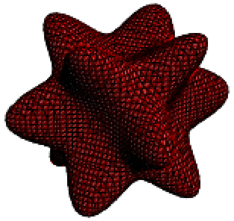
Hole mobility

Electrons vs. holes

Electrons



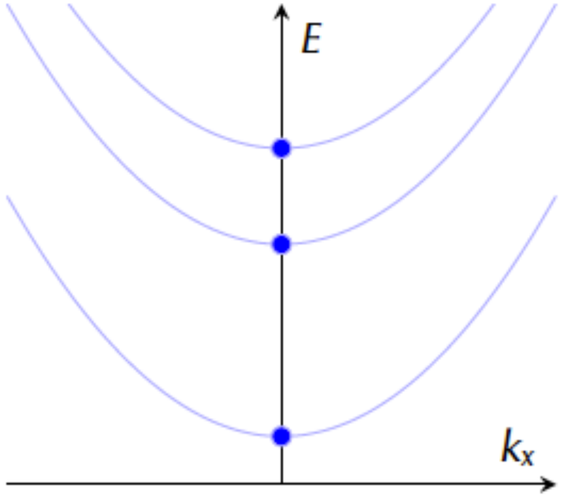
Holes



Electrons	Holes
1D quantum confinement	
separable	not separable
1 eigenvalue equation	N eigenvalue equations
$E = E_\nu + E(k_x, k_y)$	$E = E_\nu(k_x, k_y)$
Subband dispersion	
analytic	interpolation needed

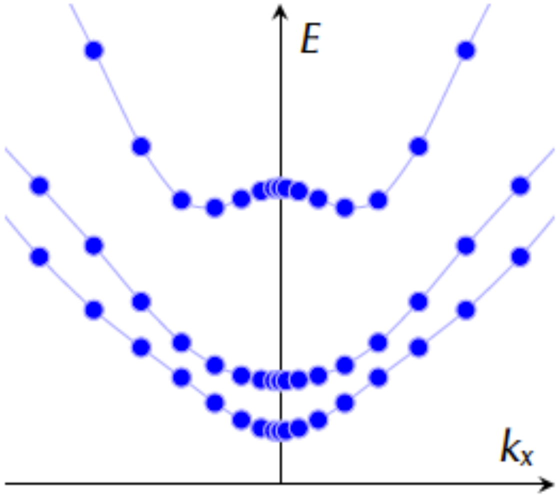
Hole mobility

Electrons



$$E = E_i + \frac{\hbar^2 k_x^2}{2m_x}$$

Holes



interpolation: $E = E_i(k_x)$

Effective mass

parameter

to be computed
depends on potential well

Hole mobility

Transport mass

Given subband i and direction α:

$$\boxed{\frac{1}{m_i^\alpha} = \frac{1}{\hbar^2}\frac{\partial^2 E_i(k)}{\partial k_\alpha^2}}$$

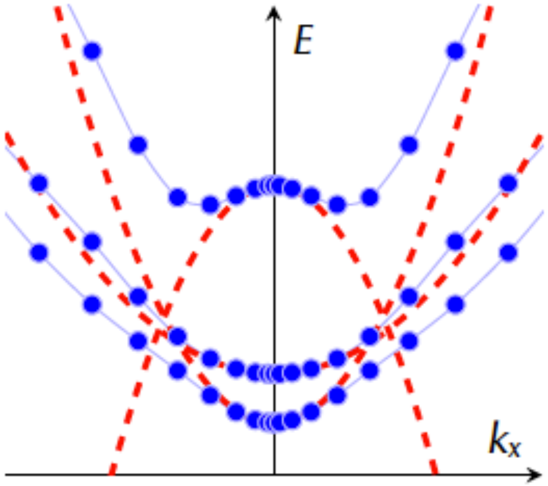
- non-parabolic:

  m_i^α depends on k

- if we take m_i^α at $k = 0$:

  parabolic approximation

  however . . .



Hole mobility

$\mathbf{k}\cdot\mathbf{p}$ method

The $\mathbf{k}\cdot\mathbf{p}$ method

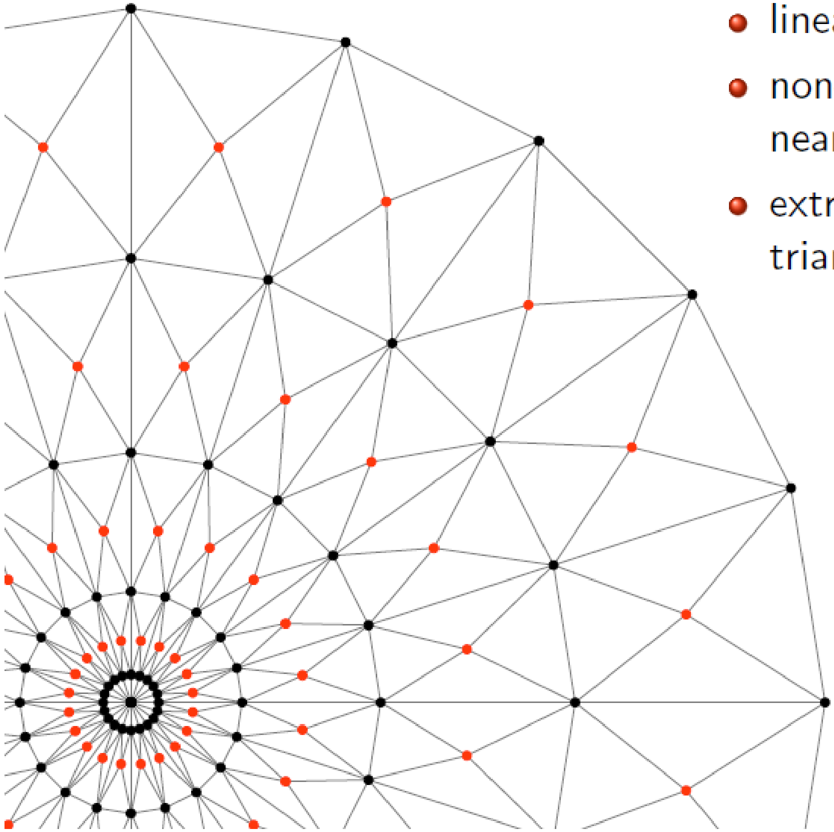
- approximate expression for the computation of band structure around $\mathbf{k} = \mathbf{k}_0$.
- an arbitrary number of bands can be considered

The valence band(s)

- degeneration (3 valence bands)
- spin-orbit interaction
- 6×6 $\mathbf{k}\cdot\mathbf{p}$ method

Hole mobility in inversion layers

The mesh (in $\mathbf{k}_{\parallel}$ plane)



- linear interpolation
- non-uniform *k*-mesh, finer near the origin
- extra points to create a triangulation

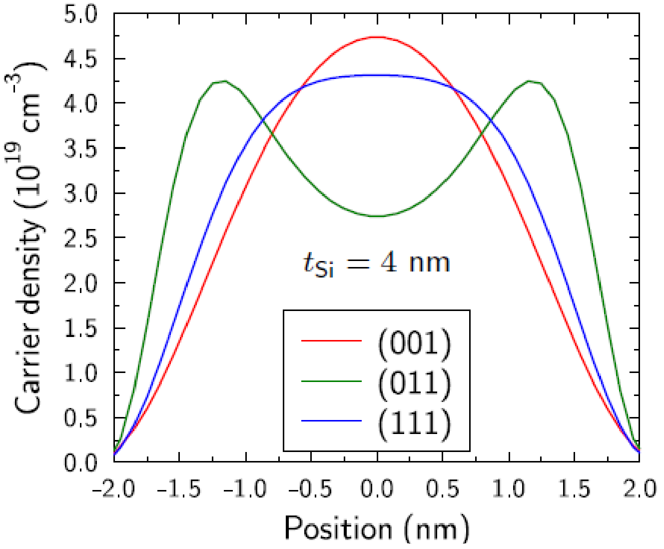
discretization

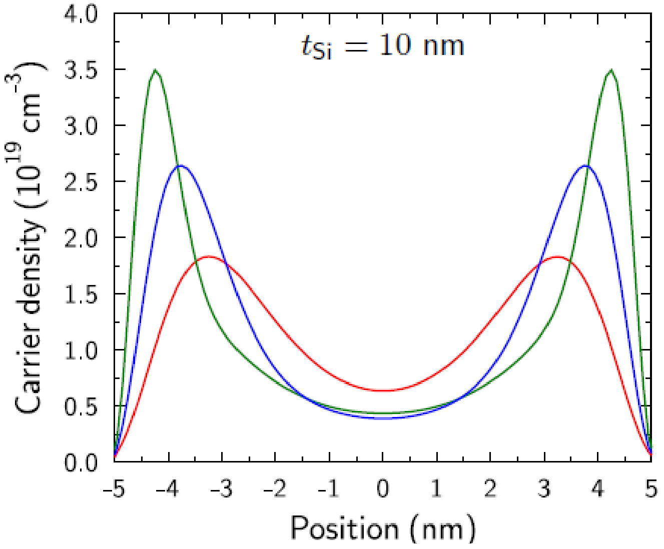
Hole mobility in DGSOI transistors

Results: inversion charge

Charge distribution

- different distance from the interface (centroid)
- one or two peaks can be present
- volume inversion can have different effects



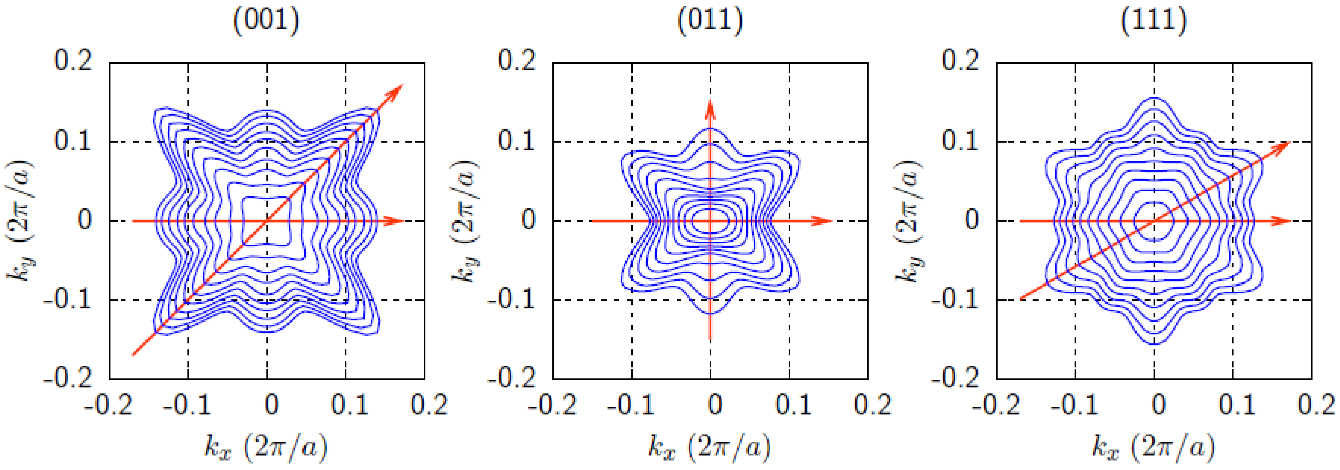


Hole mobility in DGSOI transistors

Results: energy dispersion

Energy dispersion of first subband (10 nm)

- isotropic mobility: (001) and (111) surfaces
- non-isotropic mobility: (011) surface

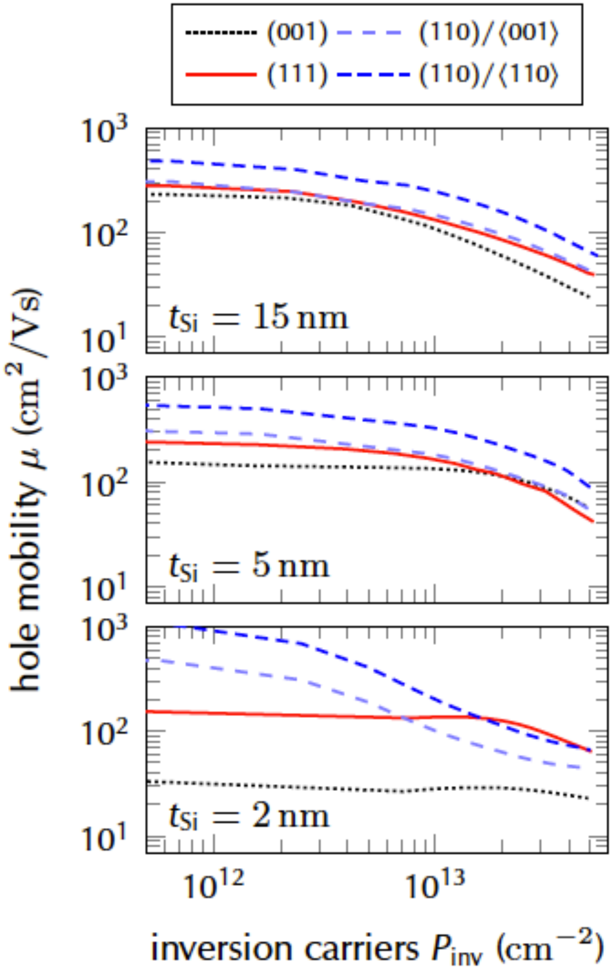


Hole mobility in DGSOI transistors

Results: hole mobility

Mobility vs. inversion charge

- negligible dependence on channel direction for (100) and (111)
- strong dependence on channel direction for (110)
- weak dependence on P_{inv} at small t_{Si} (but not for (110))
- enhancement factor of (110) and (111) increases at small t_{Si}

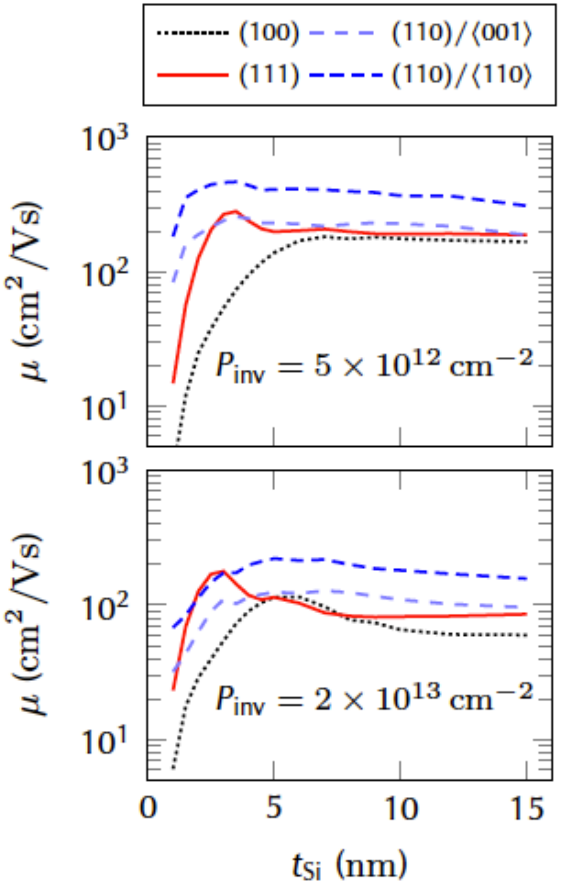


Hole mobility in DGSOI transistors

Results: hole mobility

Mobility vs. t_{Si}

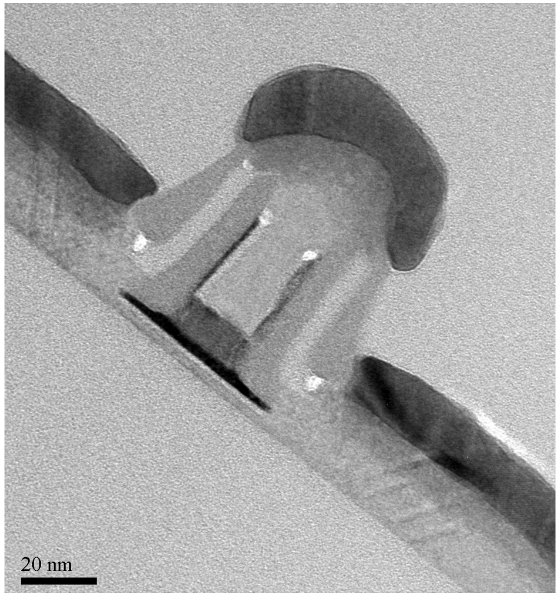
- strong mobility reduction as small t_{Si} in every case
- for (110) and (111) surface the reduction happens at smaller t_{Si}
- performance improvement of (110) and (111) increases at small t_{Si}



CMOS Scaling

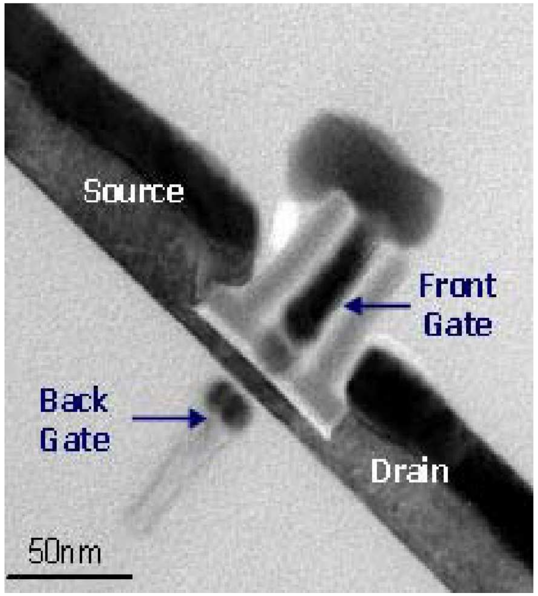
- **SOI: Thickness based & number of gates**

(Courtesy of LETI)



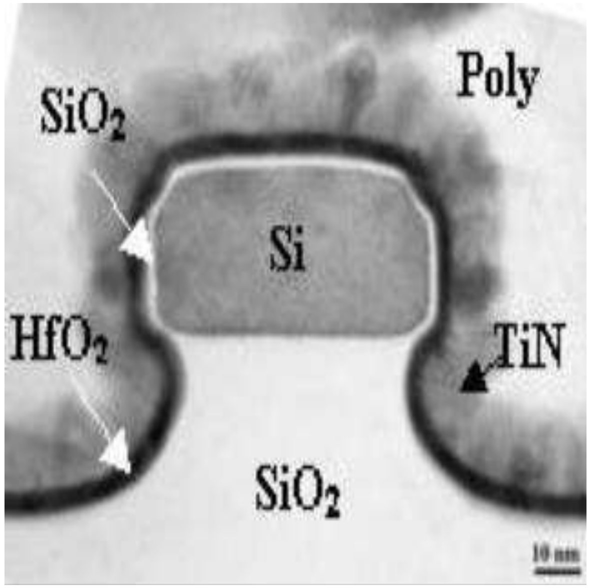
Planar FDSOI

$T_{Si} \approx L_G/4$



Double gate SOI

$T_{Si} \approx L_G/2$

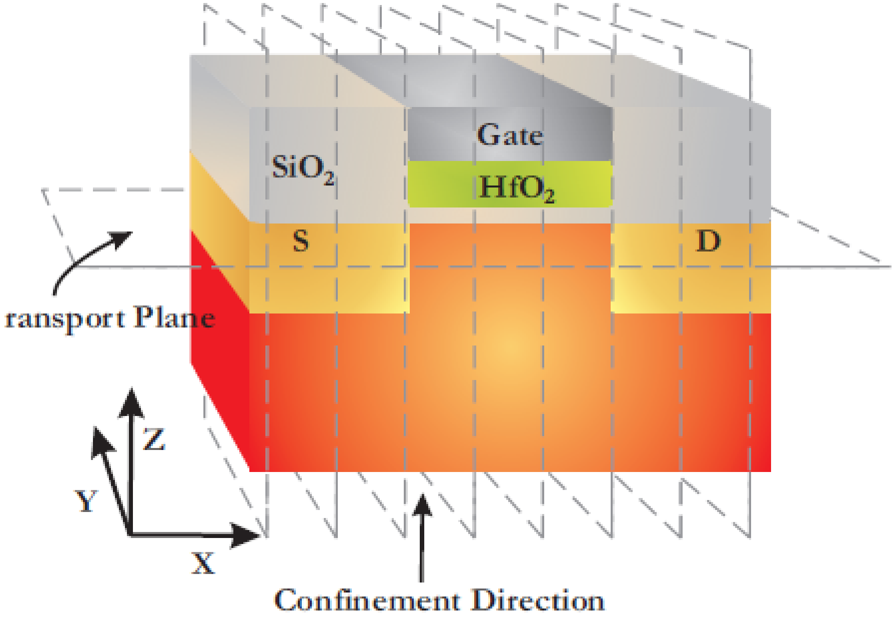


Tri-Gate/FinFET

$T_{Si} \approx W \approx L_G$

Multi-subband Monte Carlo simulation

Based on the space-mode approximation [Venugopal et al 2002]



Boltzmann Transport Equation

$$\frac{\partial f}{\partial t} + \frac{\vec{p}}{m} \cdot \nabla_{\vec{r}} f + \vec{F} \cdot \nabla_{\vec{p}} f = \left.\frac{\partial f}{\partial t}\right|_{coll}$$

Poisson's Equation

$$\nabla \left(\varepsilon \nabla V(x,z) \right) = -\rho(x,z)$$

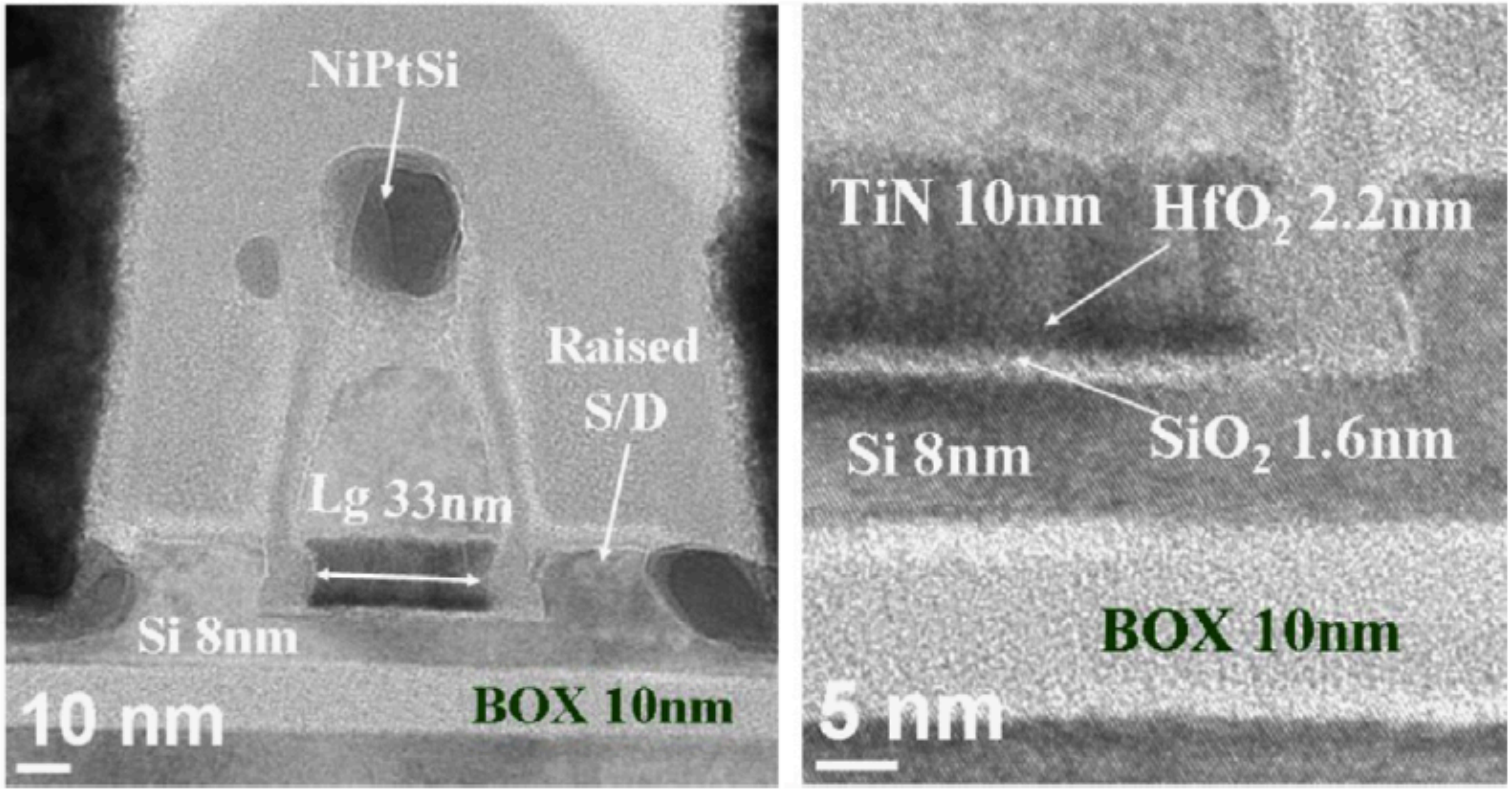
Schrödinger Equation

$$-\frac{\hbar^2}{2m_z^*} \frac{\partial^2}{\partial z^2} \Psi_j(z) - qV(z)\Psi_j(z) = E_j \Psi_j(z)$$

Multi-subband Monte Carlo simulation

Model Validation

From C. Fenouillet-Beranger et al, SSE 54 (2010) 849–854



Multi-subband Monte Carlo simulation

Model Validation

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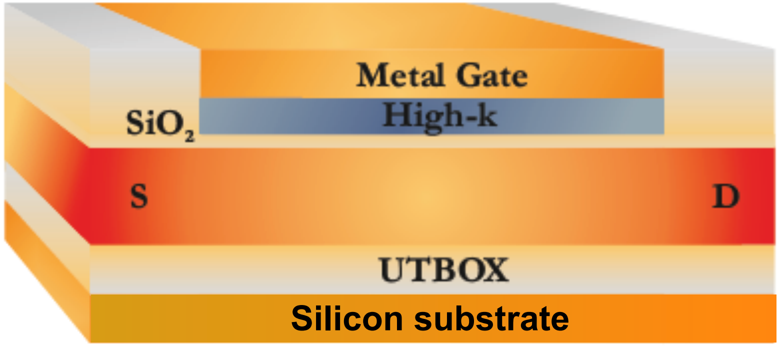
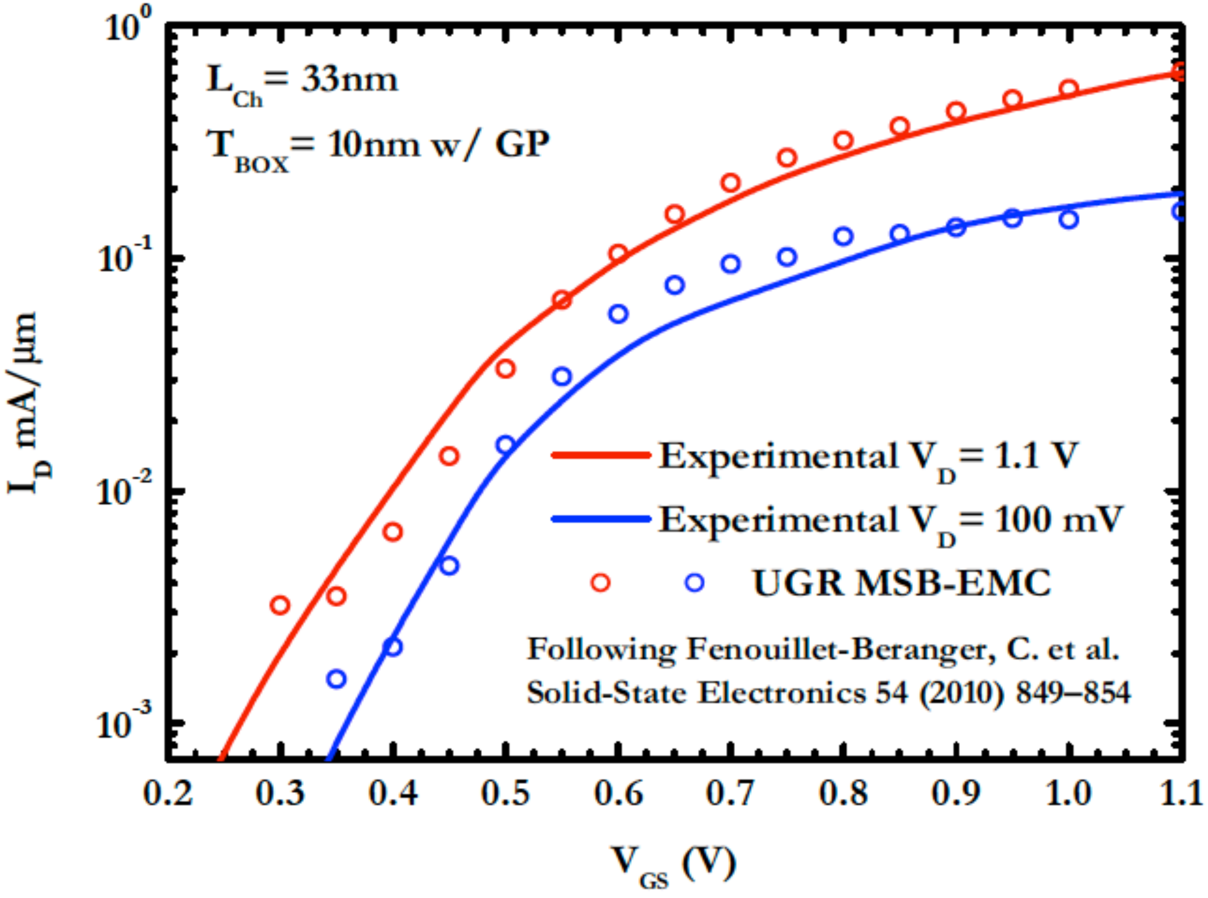


- ✧ L_G=33nm
- ✧ Midgap metal gate
- ✧ $T_{high\text{-}k}$ =2.2nm
- ✧ T_{SiO2}=1.6nm
- ✧ T_{si} = 8nm
- ✧ Lightly doped channel
- ✧ Gaussian doping profiles in S/D
- ✧ T_{BOX}=10nm

Multi-subband Monte Carlo simulation

Model Validation

From C. Fenouillet-Beranger et al, SSE 54 (2010) 849–854



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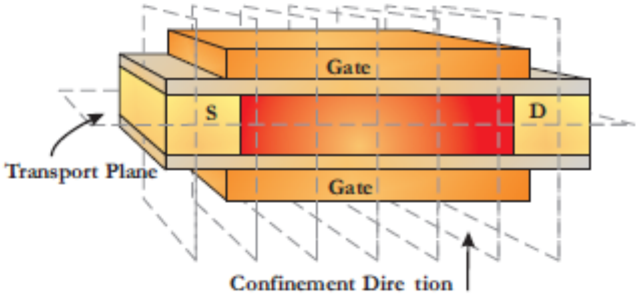
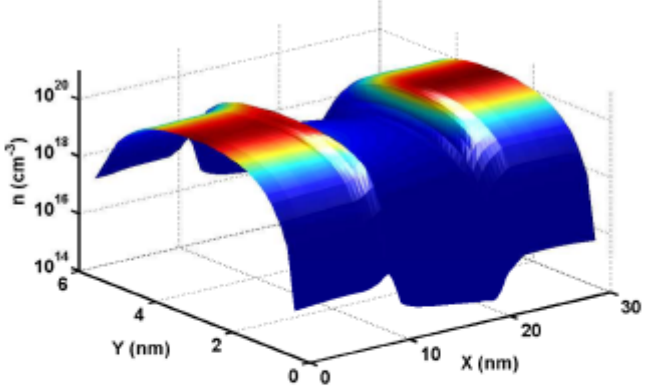
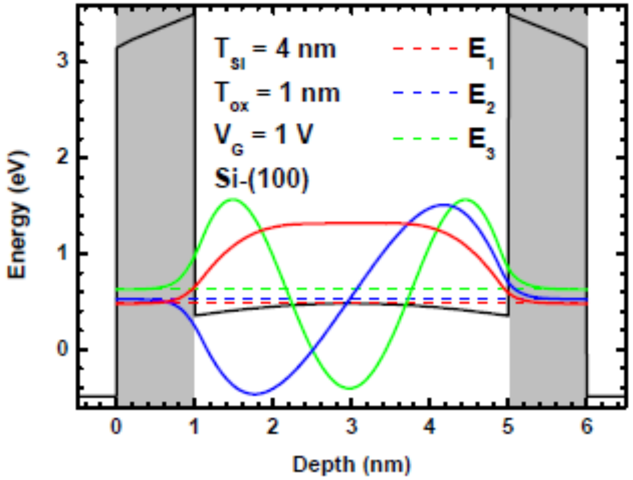
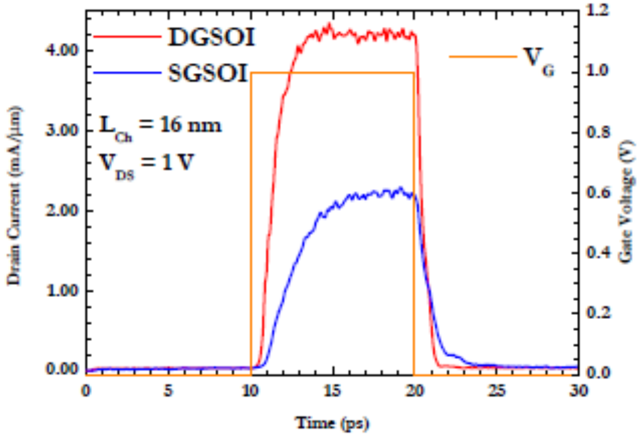
Multi-subband Monte Carlo simulation

FDSOI, DGSOI, VMT including steady state and transient simulations



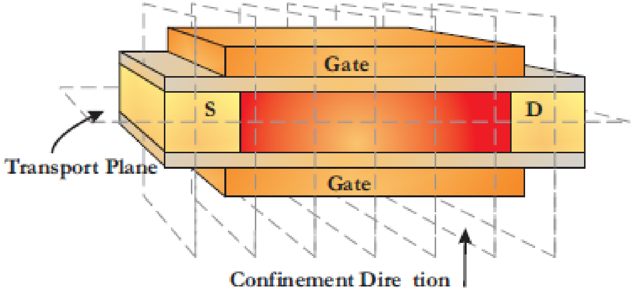


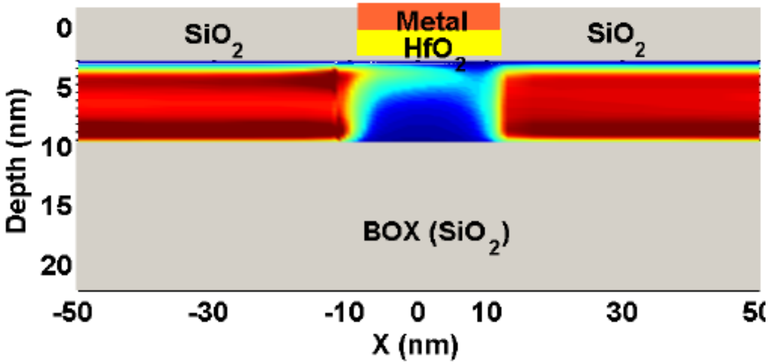


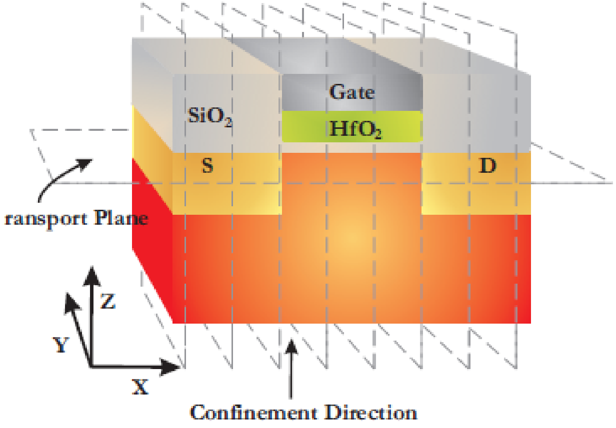


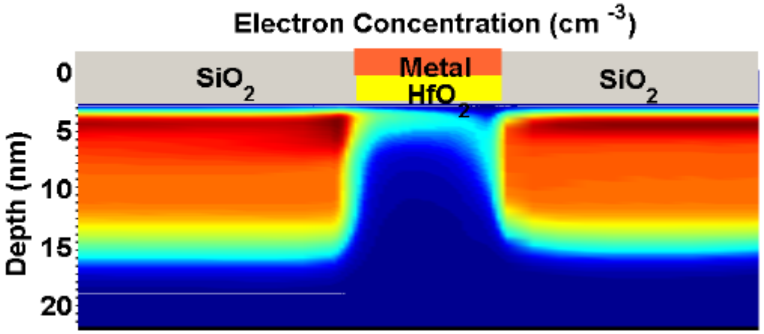
Multi-subband Monte Carlo simulation

Charge distribution along the channel:
SOI versus Bulk









Outline

A. Carrier transport properties in DGSOI
    1. Volume inversion.
    2. Electron mobility.
    3. Crystallographic orientation.
    4. Strained channels.
    5. Hole mobility.

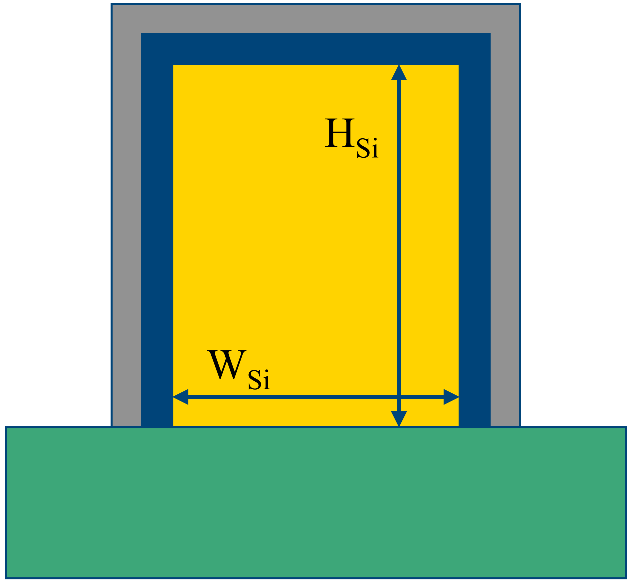
B. Ensemble Monte Carlo simulation
    1. Quantum corrections.
    2. Multisubband Monte Carlo simulations

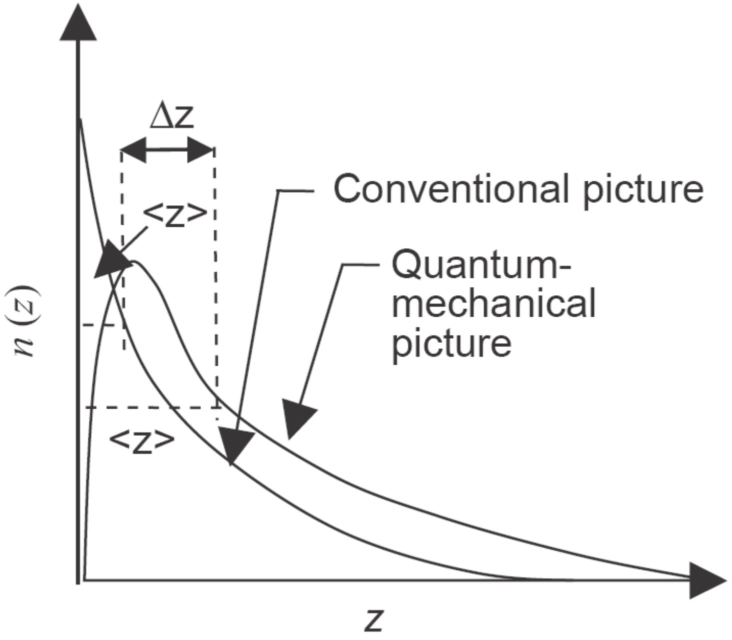
C. Multigate nanowires

Multigate transistors

Silicon substrate in the nanometer range

$H_{Si} = W_{Si} < 20\text{nm}$



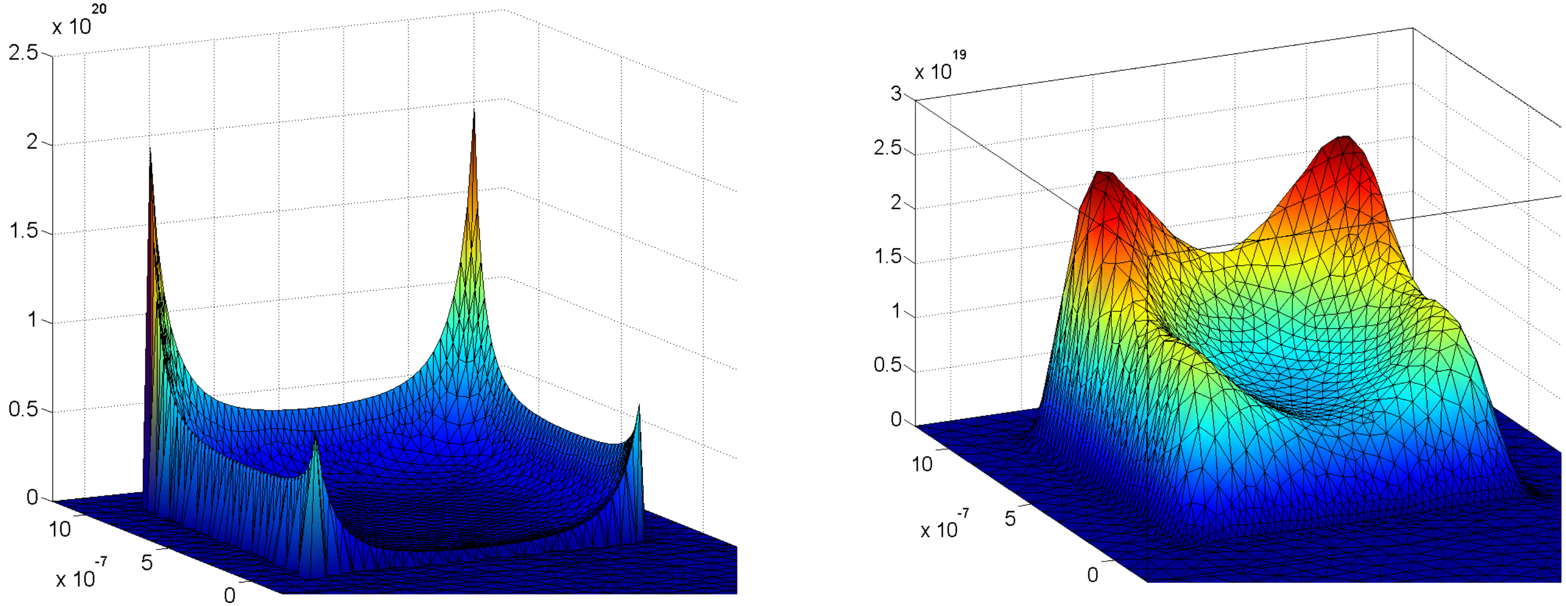


Multi-Gate transistors: 2D confinement

MUGate:Quantum effects

Electron Distribution in a Trigate MOSFET

$H_{Si} = W_{Si} = 10\text{nm}$; $T_{ox} = 2\text{nm}$; $V_G = 1\text{V}$



Classical

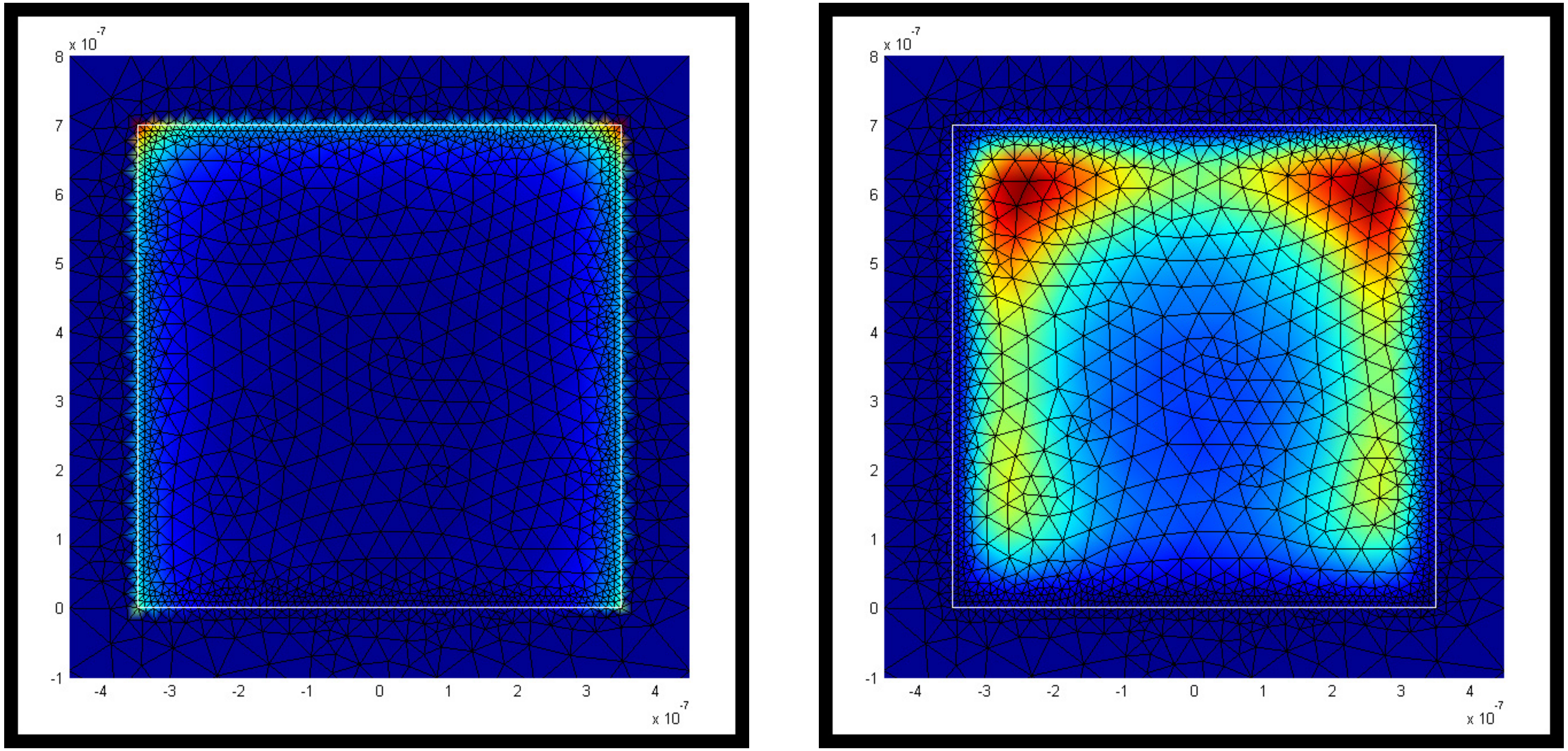
$n_{max} = 2 \times 10^{20} \text{cm}^{-3}$

Quantum

$n_{max} = 2.5 \times 10^{19} \text{cm}^{-3}$

MUGate:Quantum effects

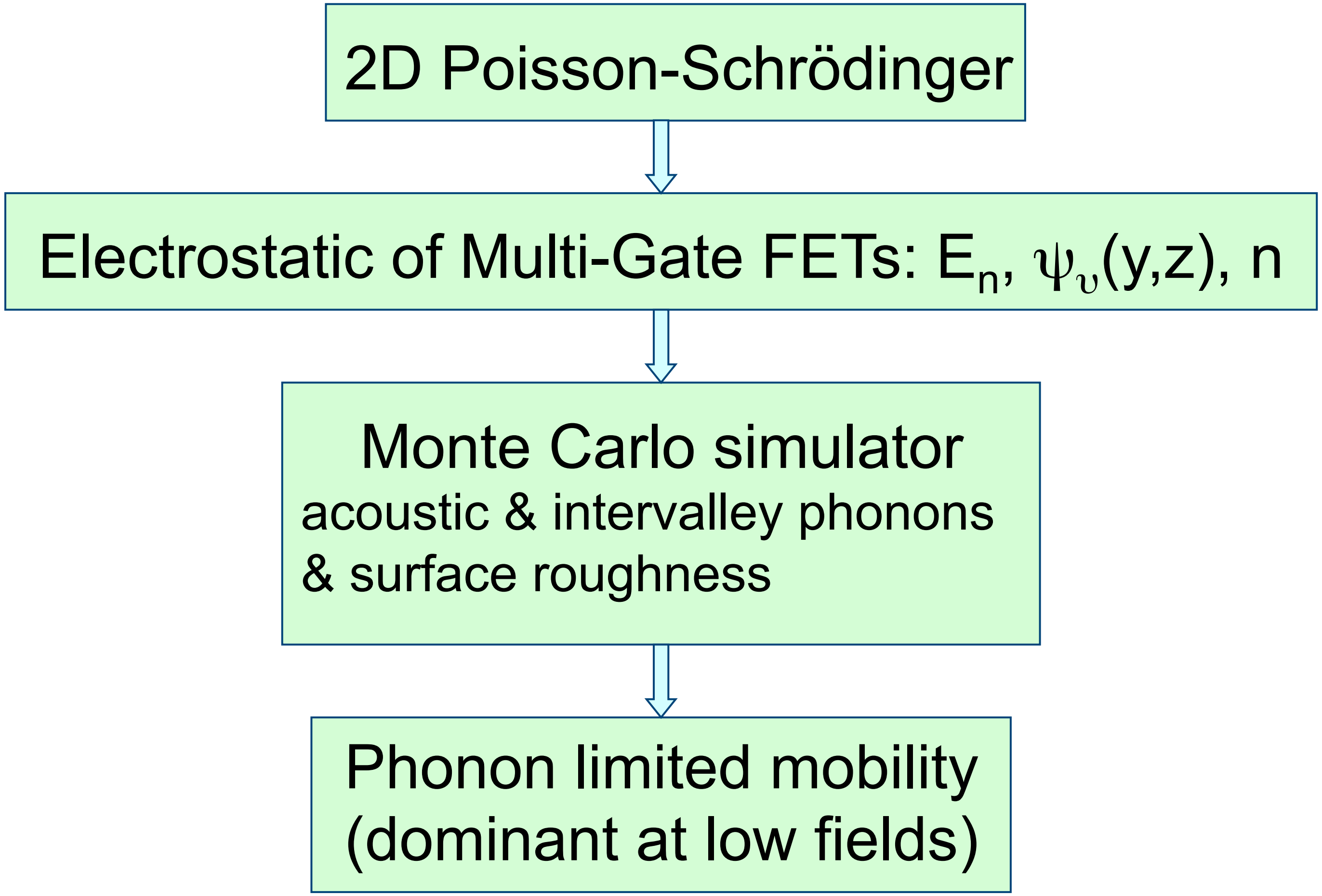
Top view of the electron distribution in a Trigate MOS



Classical

Quantum

MUGate:1D Electron transport



2D Poisson-Schrödinger

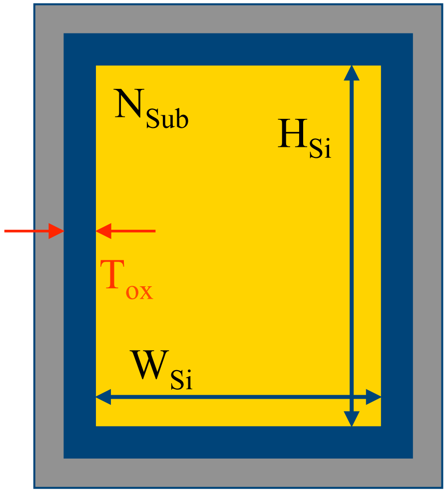
Electrostatic of Multi-Gate FETs: E_n, $\psi_\upsilon(y,z)$, n

Monte Carlo simulator
acoustic & intervalley phonons
& surface roughness

Phonon limited mobility
(dominant at low fields)

MUGate:1D Electron transport

Device under study: Quantum Wire with square cross section $H_{Si} = W_{Si}$ and different crystallographic orientations



$H_{Si} = W_{Si} = 15nm; 10nm; 5nm$

Gate voltage = [0.2, 1.5]V

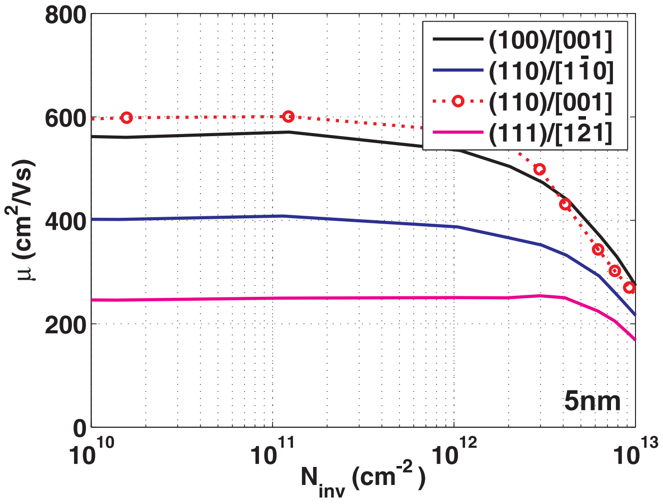
Undoped substrate, $\phi_m = 4.61eV$

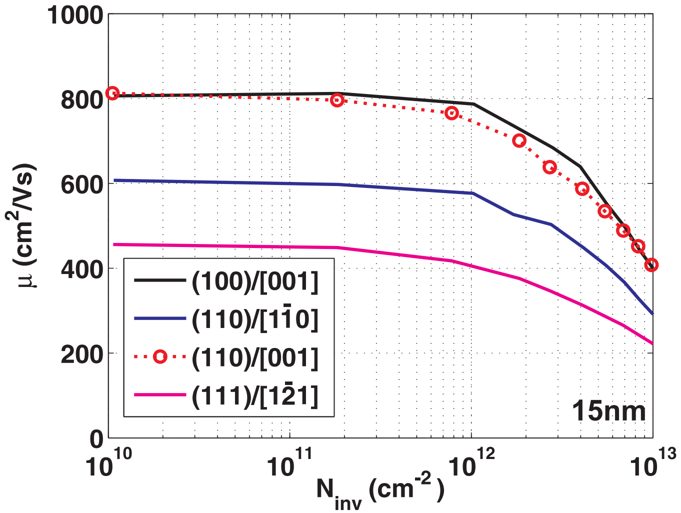
Energy values & Wave functions necessary to get 95% of the total charge → $H_{Si} = W_{Si} > 15nm$ → High number of E_n & $\psi_\upsilon(y,z)$.

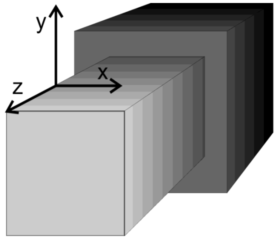
MUGate:1D Electron transport

- Phonon-limited mobility in a square wire with different orientations (YZ-plane)/[z-direction]:

There is a strong dependence on the size and on the orientation



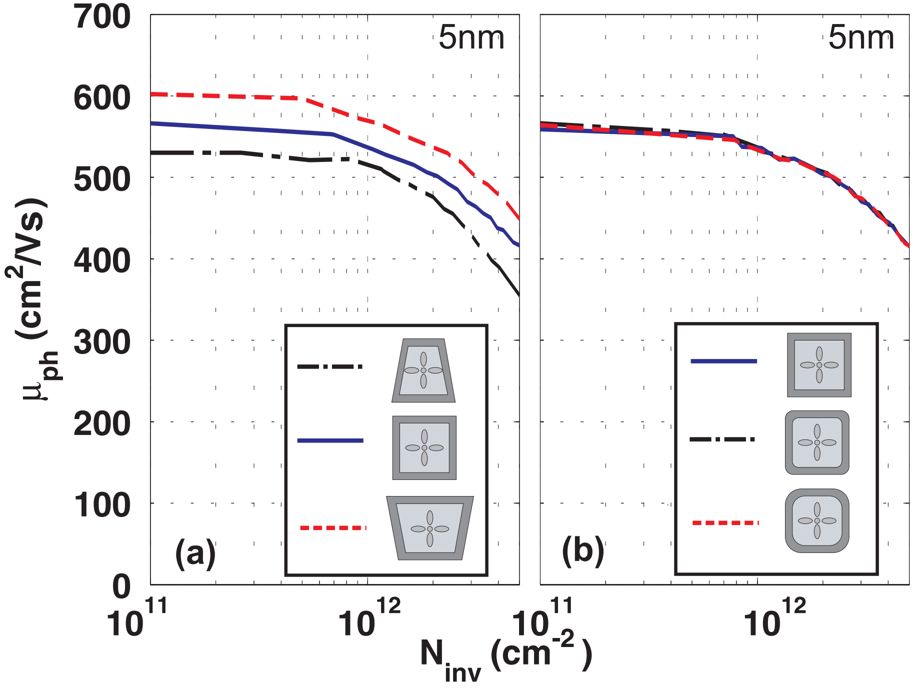


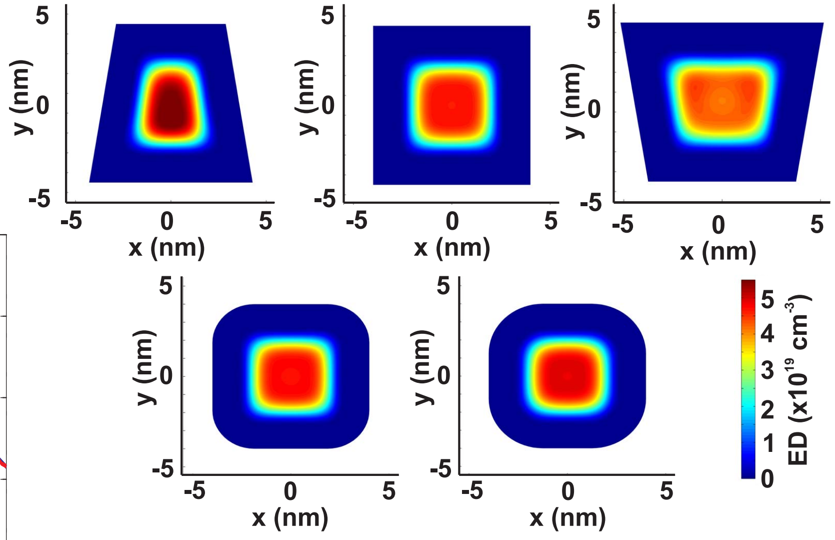


MUGate:1D Electron transport

- Phonon-limited mobility in (100)/[001] devices with different geometries:

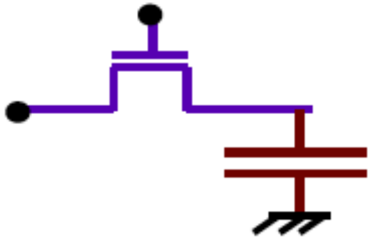
The effects of the geometry variability are more noticeable in small devices.





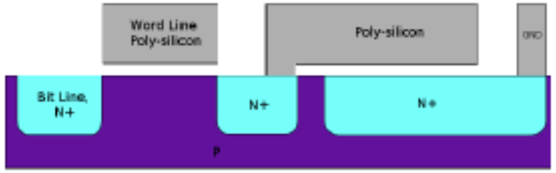
The mobility is not affected by the presence of rounding corners.

Design of 1T-DRAM cell



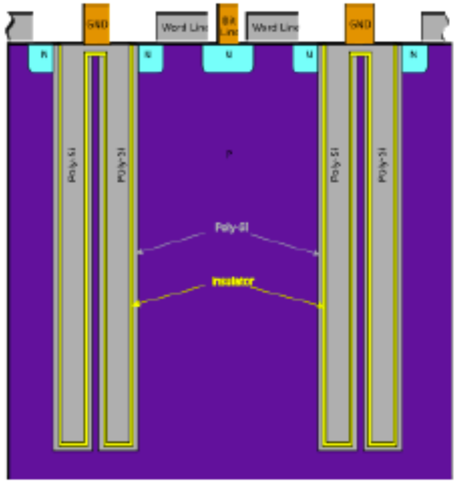
(Dennard)

DRAM in 1968



Minimum capacitance requirement
25 fF/cell

DRAM today



Standard

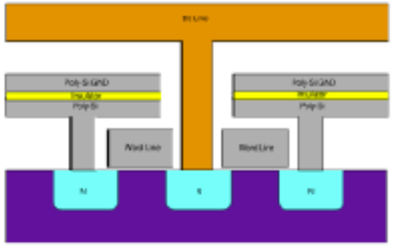
Simple concept

Complexity

Capacitance

Leakage

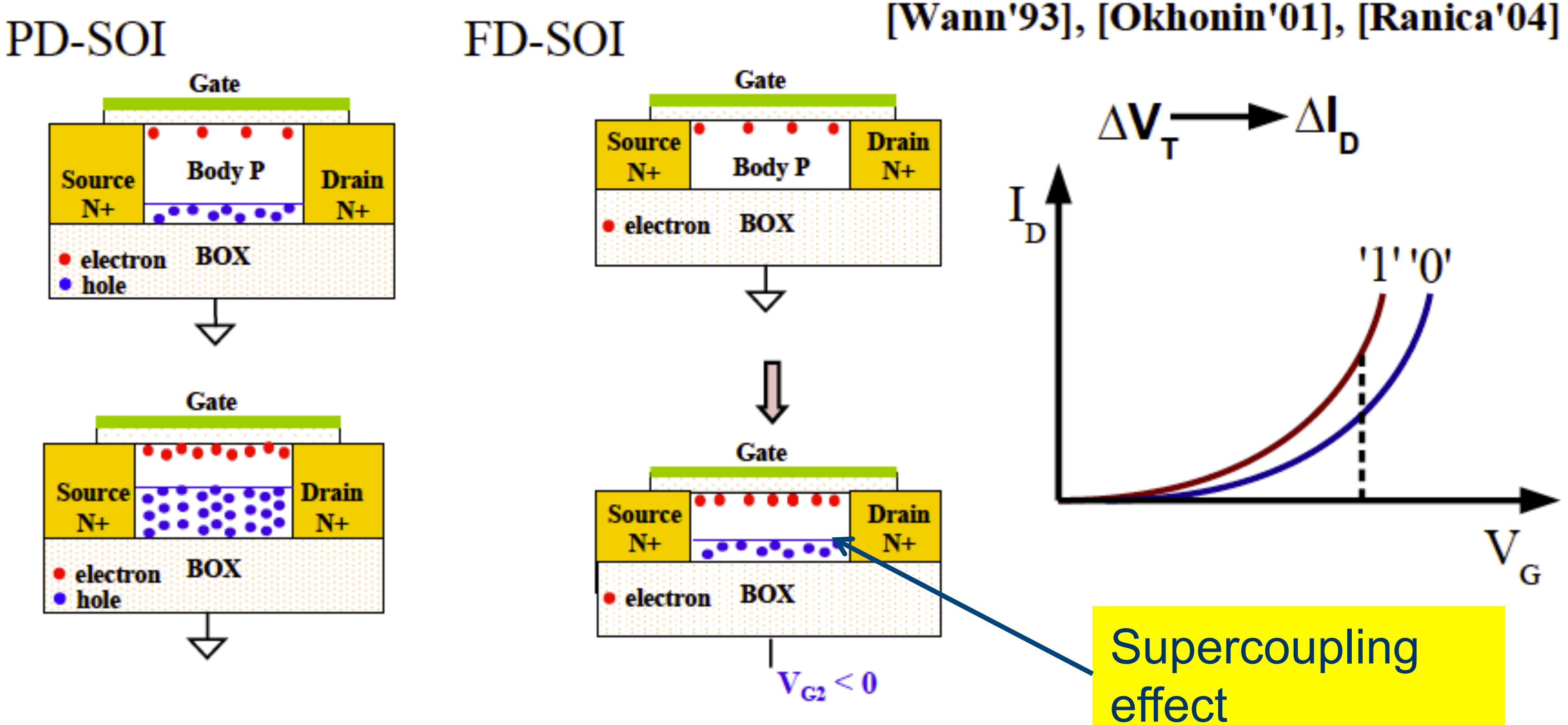
Resistance



Design of 1T-DRAM cell

The alternative: FB-1T-DRAM

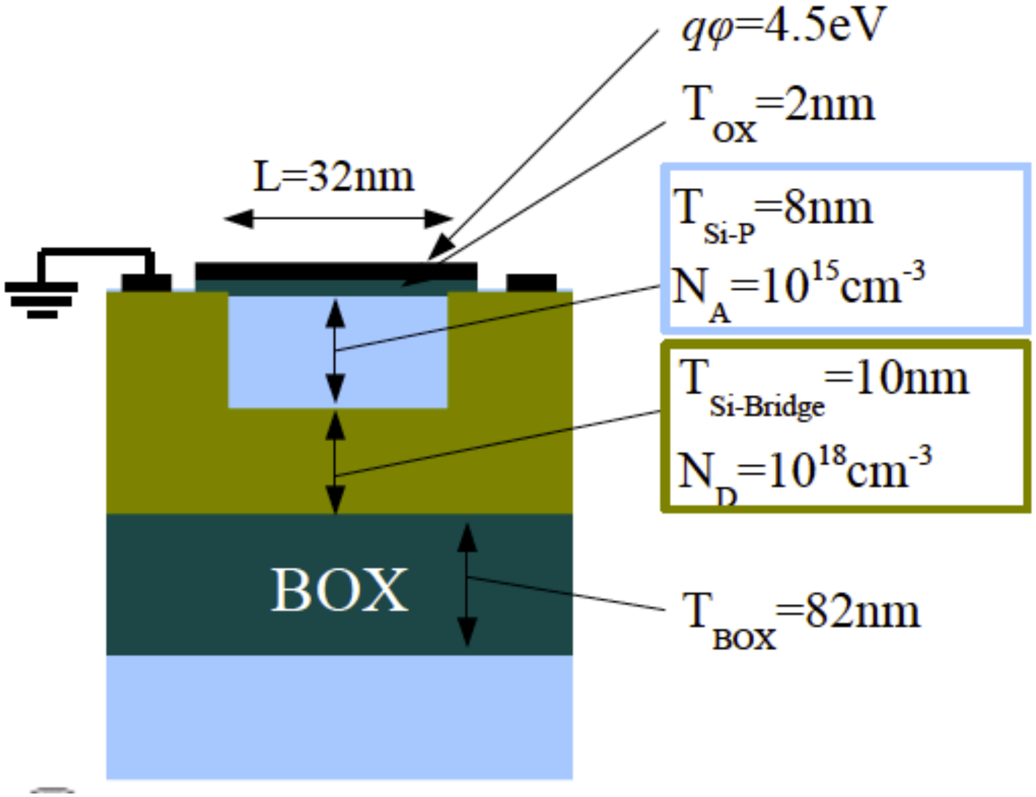
[Wann'93], [Okhonin'01], [Ranica'04]



Supercoupling effect

Design of 1T-DRAM cell

Reference Device



$q\varphi$=4.5eV

T_{OX}=2nm

L=32nm

$T_{Si\text{-}P}$=8nm

$N_A=10^{15}cm^{-3}$

$T_{Si\text{-}Bridge}$=10nm

$N_D=10^{18}cm^{-3}$

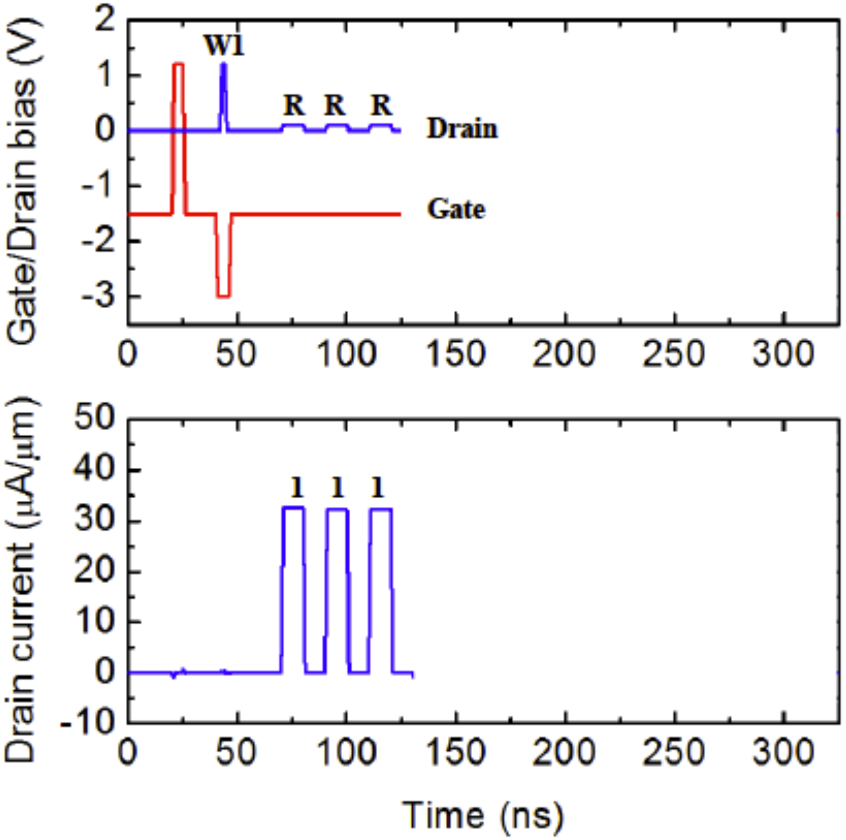
BOX

T_{BOX}=82nm

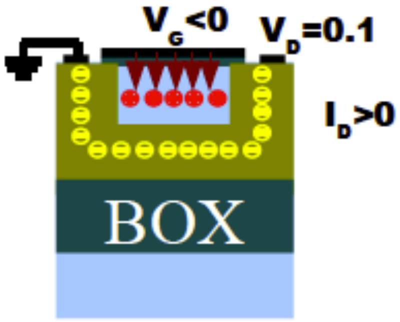
2D
SRH
Band to Band tunneling
Impact Ionization
T=25°C

Design of 1T-DRAM cell

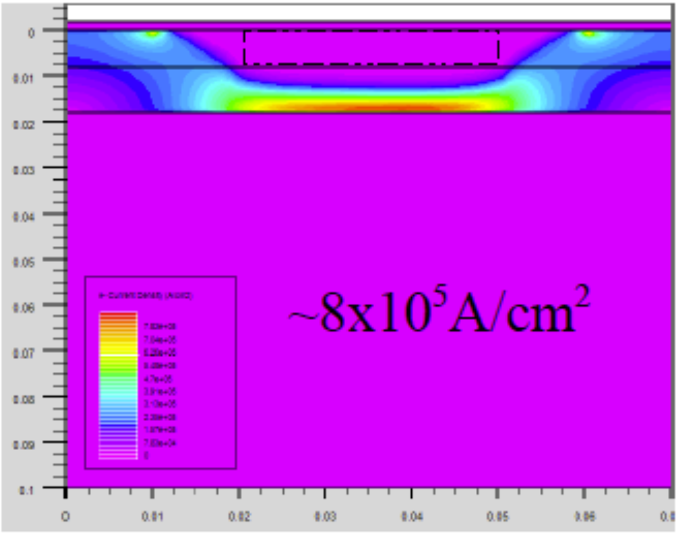
Transient simulation



Reading '1'



Electron current



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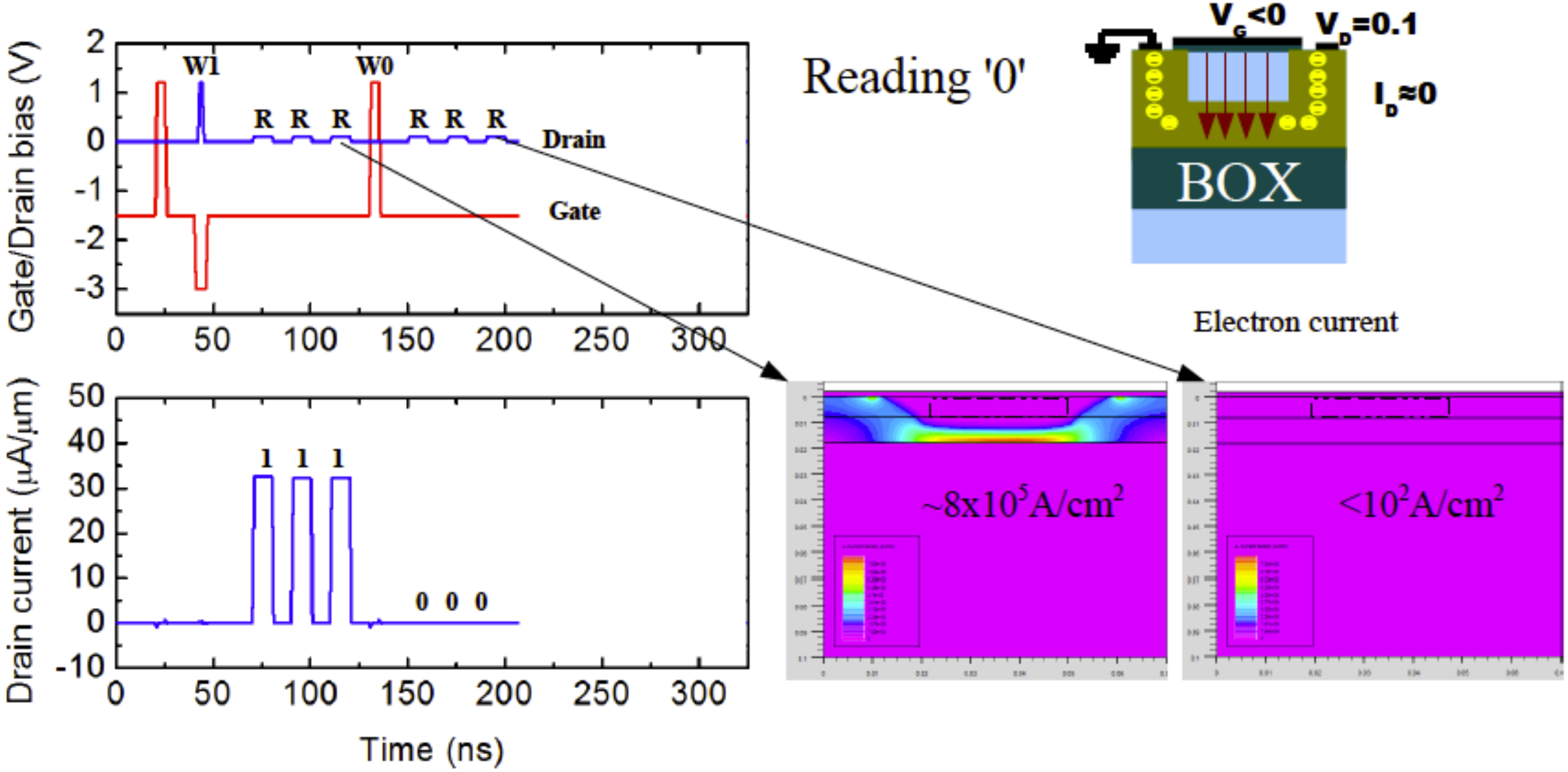
Design of 1T-DRAM cell

Transient simulation



Reading '0'

Electron current

Conclusions

- Simulation is an important and necessary tool for today’s devices.
- It’s a very complex task when you deal with real devices, but it can be faced at different complexity levels.
- It provide us with information with help us to better understand and improve our devices.

Thank you for your attention

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